Approximate Sum-of-Products Designs Based on Distributed Arithmetic

ABSTRACT:

The Approximate circuits provide high performance and require low power. Sum-of-products (SOP) units are key elements in many digital signal processing applications. In this brief, three approximate SOP (ASOP) models which are based on the distributed arithmetic are proposed. They are designed for different levels of accuracy. First model of ASOP achieves an improvement on area and on power, when compared with conventional unit. Other two models provide an improvement on area and power, respectively, with a reduced error rate compared with the first model. Third model achieves the mean relative error and normalized error distance as low. Performance of approximate units is evaluated with a noisy image smoothing application, where the proposed models are capable of achieving higher peak signal to-noise ratio than the existing state-of-the-art techniques. It is shown that the proposed approximate models achieve higher processing accuracy than existing works but with significant improvements in power and performance.

EXISTING SYSTEM:

Distributed arithmetic is a popular technique for implementing the SOP computations without the use of multipliers. SOP units based on the distributed arithmetic are frequently used in filters and other DSP applications. The main advantage of distributed arithmetic is its high computational efficiency. Distributed arithmetic distributes multiply and accumulate operations across adders, lookup tables, and final accumulation in such a way that conventional multipliers are not required.

PROPOSED SYSTEM:
proposed system leading one predictor for approximation, and provides approximation in the lower significant part. Area power tradeoff with error analysis is analyzed and it is found that our proposed models have better APP compared to exact and existing approximate designs and with lower error metrics compared to existing models.

**Applications:**

1. multimedia
2. digital signal processing

**Advantages:**

Delay and power reduced.

**System Configuration:-**

In the hardware part a normal computer where Xilinx ISE 14.7 software can be easily operated is required, i.e., with a minimum system configuration

**HARDWARE REQUIREMENT**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Pentium –III</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>1.1 GHz</td>
</tr>
<tr>
<td>RAM</td>
<td>1 GB (min)</td>
</tr>
<tr>
<td>Hard Disk</td>
<td>40 GB</td>
</tr>
<tr>
<td>Floppy Drive</td>
<td>1.44 MB</td>
</tr>
<tr>
<td>Key Board</td>
<td>Standard Windows Keyboard</td>
</tr>
</tbody>
</table>

Further Details Contact: A. Vinay 9030333433, 08772261612, 9014123891 #301, 303 & 304, 3rd Floor, AVR Buildings, Opp to SV Music College, Balaji Colony, Tirupati - 515702 Email: info@takeoffprojects.com | www.takeoffprojects.com
Mouse - Two or Three Button Mouse

Monitor - SVGA

SOFTWARE REQUIREMENTS


- Front End: Modelsim 6.3 for Debugging and Xilinx 14.7 for Synthesis and Hardware Implementation

- This software’s where Verilog source code can be used for design implementation.