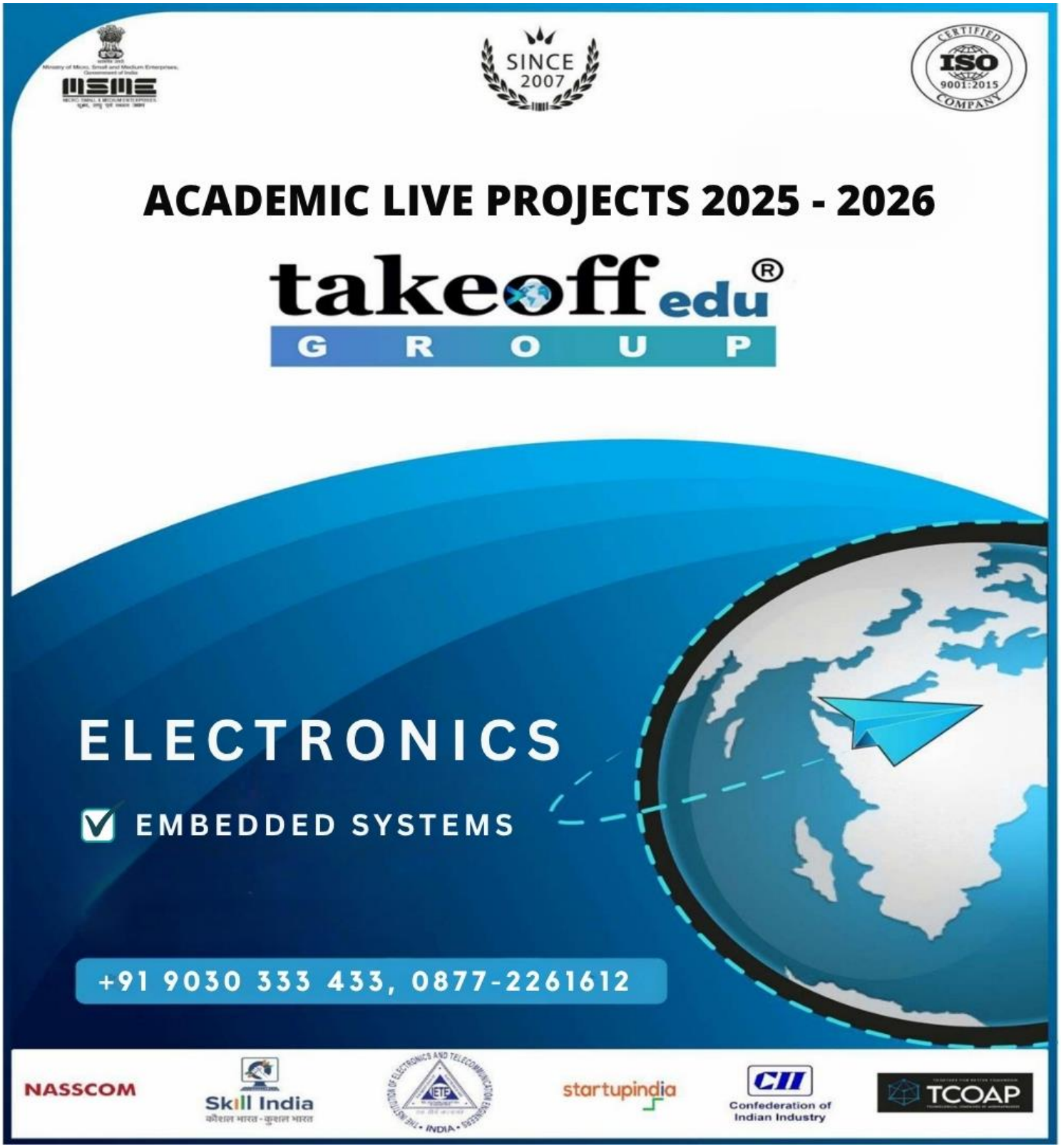
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S.No.	PROJECT CODE	TITLE	DOMAIN
1.	TEMBMA3698	**Enhanced And Light Weight Yolov8 Based Model For Accurate Rice Pest Detection** To detect rice pests using a lightweight YOLOv8 model. Aims for real-time, field-ready pest identification.	AI
2.	TEMBMA3687	**Fruit Monitoring and Harvest Date Prediction Using On-Tree Automatic Image Tracking** To monitor on-tree fruit growth-using automatic image tracking. Predicts optimal harvest dates to improve yield quality.	Deep Learning
3.	TEMBMA3693	**Low Cost, Multi Sensor Non Destructive Banana Ripeness Estimation Using Machine Learning** To estimate banana ripeness using multiple low-cost sensors. Machine learning enables accurate non-destructive analysis.	Machine Learning
4.	TEMBMA3694	**Enhancing Road Safety: Detection of Animals on Highways During Night** To detect animals on roads at night using ML and vision. Reduces collision risk and improves highway safety.	Machine Learning
5.	TEMBMA3695	**Steroid Level Detection in Milk Production** To identify steroid residues in milk using sensors and ML. Ensures dairy safety and regulatory compliance.	Machine Learning
6.	TEMBMA3734	**Development of an IoT-Enabled Smart Healthcare Monitoring System for Real-Time Patient Health Surveillance** The main objective is to develop a Smart Healthcare Monitoring System using IoT for real-time monitoring of vital signs like heart rate, temperature, and ECG via Arduino UNO and sensors. Data is displayed on an LCD, uploaded to the cloud, and alerts	Biomedical

		are sent for abnormal readings to enable remote care and early diagnosis.	
7.	TEMBMA3696	**Efficient Web Based Automated Poultry Disease Detection Using Transfer Learning Models** To detect poultry diseases from images on a web interface. Uses pretrained models for quick and accurate diagnosis.	**AI**
8.	TEMBMA3735	**AIoT-Based Meat Quality Monitoring Using Camera and Gas Sensor With Wireless Charging** To evaluate meat freshness using gas sensors and cameras. Wireless charging powers real-time AI-based analysis.	**IOT**
9.	TEMBMA3700	**Automated Disease Detection in Oyster Mushroom Cultivation Using Deep Learning Technique** To develop a deep learning-based system for detecting diseases in oyster mushrooms using image data. The goal is to enable early diagnosis and improve yield quality in mushroom farming.	**Deep Learning**
10.	TEMBMA3736	**IoT and ML for Air Pollution Monitoring with Real Time Data and Prediction of Health Advisory** The main objective is to develop an IoT and ML-based system for real-time air pollution monitoring using sensors at traffic signals to track CO, CO_2, and smoke levels. It analyzes data with a Decision Tree Classifier to provide health advisories, safe travel routes, and personalized recommendations via a mobile app.	**Machine learning**
11.	TEMBMA3737	**Real-Time GPS Tracking and Health Monitoring for Animals Using IoT and Mobile Application** The main objective is to develop an IoT-based real-time GPS and health monitoring system for animals to track location and heart rate using GPS and heartbeat sensors. Data is sent to a mobile app for live monitoring, with alerts on abnormal heart rates to support timely health interventions and prevent theft.	**IOT**
12.	TEMBMA3738	**IoT-Enhanced Battery Management System: Real-Time Monitoring, Predictive Analytics and Safety Optimization**	**IOT**

		The main objective is to develop an IoT-based Battery Management System for real-time monitoring and control of battery parameters using sensors, cloud integration, and machine learning. It enhances safety, efficiency, and longevity while enabling predictive analytics to reduce maintenance costs and promote sustainable battery usage.	
13.	TEMBMA3739	**Electric Vehicle Battery Parameters Monitoring System using IoT** The main objective is to develop an IoT-based system for real-time monitoring of electric vehicle battery metrics to enhance safety and lifespan. It uses predictive analytics for early warnings and optimized charging, with remote monitoring through a custom dashboard to improve performance and maintenance.	**IOT**
14.	TEMBMA3699	**IoT-Based Traffic Prediction for Smart Cities** To collect and predict urban traffic using IoT and ML. Optimizes mobility and smart city planning.	**IOT**
15.	TEMBMA3703	**Pothole Detection Using Deep Learning Classification Method** To develop a deep learning-based classification model for detecting potholes in road images. The goal is to support timely maintenance and enhance transportation safety.	**Deep Learning**
16.	TEMBMA3757	**Yolo-Early Fire/Smoke Detection Using Deep Learning Yolo** To build a YOLO-based model for fast and accurate early detection of fire and smoke. The aim is to enable real-time alerts for improved safety and disaster prevention.	**Deep Learning**
17.	TEMBMA3741	**Plant Leaf Detection and Disease Recognition using Deep Learning** To develop a deep learning model that detects plant leaves and identifies diseases from images. The goal is to support early diagnosis and improve crop yield through automation.	**Deep Learning**
18.	TEMBMA3742	**IoT-Based Gas Leak Detection and Fire Hazard Recognition System Using Image Processing for Household Safety Enhancement**	**IOT**

		The main objective is to develop an IoT-based system for early detection of gas leaks and fire hazards with real-time monitoring and automatic gas shutoff. It enhances household safety by sending instant emergency alerts	
19.	**TEMBMA3688**	**A Review of Metal Surface Defect Detection Technologies in Industrial Applications** To analyze technologies for detecting defects on metal surfaces. Focus is on AI trends in industrial quality control.	**Deep Learning**
20.	**TEMBMA3692**	**Work Place Safety: Machine Learning Techniques for Assessing Workplace Incident Severity** To assess workplace risk severity using machine learning. Helps in proactive safety planning and prevention.	**Machine Learning**
21.	**TEMBMA3743**	**ATMASAWADAHASTA: An Assistive Communication Device for Mobility and Speech-Impaired Patients** The main objective is to create a wearable glove that helps mobility and speech-impaired individuals communicate using touch sensors and text-to-speech technology.	**OpenCV**
22.	**TEMBMA3744**	**Hand Gestures Mechanism for Controlling and Supervising the Smart Mattress** The main objective is to develop a smart mattress system that adjusts bed positions using hand gestures for easier control, especially for disabled patients. It also monitors vital signs and sends alerts to doctors to improve patient safety and comfort.	**Biomedical**
23.	**TEMBMA3745**	**Satellite-Based Forest Stand Detection Using Artificial Intelligence** To detect and classify forest stands using satellite imagery. AI helps automate and scale forest monitoring.	**AI**
24.	**TEMBMA3707**	**A Low Computational Cost Deep Learning Approach for Localization and Classification of Diseases and Pests in Coffee Leaves**	**Deep Learning**

		To classify pests and diseases on coffee leaves efficiently. Uses low-resource DL models for remote areas.	
25.	TEMBMA3746	**Water Leakage Detection and Recognition System** The main objective is to develop an IoT-based system that detects water leaks in real-time using sensors and machine learning for accurate prediction. It aims to send quick alerts to users to prevent water loss and improve leak management.	**Machine learning**
26.	TEMBMA3747	**IoT Enabled Device-to-Device Communication for Smart City Application** The main objective is to create an IoT system that enables direct communication between devices for smart home control, improving energy efficiency and convenience. It allows users to remotely manage appliances through a mobile app with reliable and low-latency connections.	**IOT**
27.	TEMBMA3748	**Low-Cost, Multisensor Nondestructive Banana Ripeness Estimation Using Machine Learning** The main objective is to develop a low-cost, nondestructive system to estimate banana ripeness using multiple sensors and machine learning. It aims to provide quick and accurate ripeness detection to improve fruit handling and reduce waste.	**Machine learning**
28.	TEMBMA3749	**Smart Temperature Monitoring System with GPS Integration for Pharmaceutical Safety** The main objective is to develop a low-cost Arduino-based system for real-time temperature monitoring with GPS and mobile app support. It aims to ensure pharmaceutical safety by sending alerts when temperatures cross set limits.	**Embedded Applications**
29.	TEMBMA3750	**Design of Intelligent Wardrobe System Based on IoT Technology** The main objective is to design an IoT-based smart wardrobe that offers features like dehumidification, temperature and humidity monitoring, and smart lighting. It aims to help users	**IOT**

		organize clothes easily, prevent mildew, and get daily outfit suggestions.	
30.	**TEMBMA3751**	**Design and Implementation of an IoT-Enabled Rover with ESP32 CAM for Object Detection, Environmental Monitoring, and Web-Based Control** The main objective is to design an IoT-enabled rover using ESP32-CAM for object detection and environmental monitoring. It aims to provide real-time data and remote control for uses like farming, surveillance, and disaster response.	**IOT**
31.	**TEMBMA3714**	**IVEMPS: IoT-Based Vehicle Emission Monitoring and Prediction System** The main objective is to develop an IoT-based system that monitors and predicts vehicle emissions in real time using gas sensors and deep learning. It aims to identify high-emission vehicles early and support pollution control through a web-based dashboard.	**IOT**
32.	**TEMBMA3752**	**RF and IoT-Driven Automated Lane Clearance System for Enhanced Emergency Response** The main objective is to develop an automated lane clearance system using RF and IoT technologies that enables real-time communication between ambulances, vehicles, and traffic signals. This system aims to clear traffic paths quickly and control signals to reduce ambulance response times and improve emergency services in congested urban areas.	**IOT**
33.	**TEMBMA3753**	**Utilization of Li-Fi Technology for Black Box in Ground Vehicles** The objective is to develop a low-cost, universal Black Box for vehicles using Li-Fi technology to enable fast data communication for accident analysis, safety improvement, and quicker emergency response. The system also facilitates car-to-car communication to detect collision risks early, enhancing road safety and aiding insurance and medical processes.	**WSN**
34.	**TEMBMA3690**	**Plant Disease Classification Using an Ensemble Learning Model of Convolutional Neural Networks and Vision Transformers**	**Deep Learning**

		To combine CNN and ViT for robust plant disease detection. Boosts accuracy and adaptability in agriculture.	
35.	TEMBMA3754	**Intelligent Energy-Efficient GNSS-Assisted and LoRa-Based Positioning for Wildlife Tracking** The objective is to develop an energy-efficient wildlife tracking system using LoRaWAN modules to collect RSSI and SNR data, combined with GNSS modules for occasional position updates, and use trajectory information for accurate location estimation. This system aims to balance precise tracking with low power use to extend monitoring time.	**WSN**
36.	TEMBMA3758	**Enhancing Care and Communication for Paralyzed Patients: A Microcontroller-Based Gesture Sensor Approach with GSM Integration** The project uses a microcontroller with gesture sensors to detect hand movements from paralyzed patients and sends alerts through a GSM module for easy communication. This system helps improve patient care by enabling quick and reliable emergency notifications.	**Embedded Applications**
37.	TEMBMA3755	**Web-Server Controlled Rover with Robotic Arm and Object Detection** The objective is to design a web-server controlled rover with a robotic arm that allows remote movement and object detection using camera modules. This system enables real-time control and monitoring for efficient automation and interaction.	**Robotics**
38.	TEMBMA3756	**A Real-Time Intelligent System Based on Machine-Learning Methods for Improving Communication in Sign Language** The objective is to develop an intelligent system using a camera and machine learning to accurately recognize and translate sign language gestures into text or speech. This helps improve communication for people who use sign language.	**Machine-Learning**
39.	TEMBMA3709	**A Portable Real-Time Electronic Nose for Evaluating Seafood Freshness Using Machine Learning**	**Machine Learning**

		To detect seafood freshness using gas sensors and ML. Offers portable, real-time spoilage prediction.	
40.	**TEMBMA3710**	**Fast and High-Precision Human Fall Detection Using Improved YOLOv8 Model** To detect human falls quickly using an optimized YOLOv8. Provides real-time alerts in care or surveillance systems.	**AI**
41.	**TEMBMA3759**	**YOLO-Based Abnormal Behavior Detection System for Elderly Healthcare Monitoring** The objective of this system is to use YOLO-based computer vision to accurately detect abnormal behaviors in elderly individuals. It ensures timely alerts for caregivers, promoting safety and continuous healthcare monitoring.	**Deep Learning**
42.	**TEMBMA3761**	**Smart Greenhouse Monitoring with Predictive Crop Health using ML** The objective of Smart Greenhouse Monitoring with Predictive Crop Health using ML is to create an intelligent system that monitors environmental conditions and predicts crop health using machine learning. This helps optimize growth, prevent diseases, and improve agricultural productivity.	**Machine Learning**
43.	**TEMBMA3762**	**AI Powered Automatic Pothole Detection and Filling System for Smart Road Maintenance** The objective of AI-Powered Automatic Pothole Detection and Filling System for Smart Road Maintenance is to develop an intelligent system that detects potholes in real-time using AI and automates the filling process. This ensures safer roads, reduces maintenance costs, and enhances transportation efficiency.	**Image Processing**

44.	TEMBMA3763	**Intelligent Chemical Monitoring System Using Raspberry Pi, LoRa, and Machine Learning** The objective is to build a low-cost Raspberry Pi–based system that monitors chemical parameters in real time, uses LoRa for data transmission, and applies ML to predict risks for safer chemical management.	**WSN**
45.	TEMBMA3765	**Raspberry Pi-Based Eye Movement Controlled Cursor System Using OpenCV** The objective is to create a Raspberry Pi–based system that uses OpenCV to track eye movements for hands-free cursor control, enhancing accessibility for differently-abled individuals.	**Opencv**
46.	TEMBMA3766	**AI-Powered Crop Monitoring System with Android App Integration** The objective is to build an AI-powered crop monitoring system that provides real-time health analysis and alerts via an Android app, helping farmers boost yield and manage crops effectively.	**Embedded+Android**
47.	TEMBMA3767	**Automated Weed Identification and Plucking Using Deep Learning Techniques** The objective is to create a deep learning–based system that automatically identifies and removes weeds, reducing crop damage, lowering manual effort, and improving farming productivity.	**DeepLearning**
48.	TEMBMA3793	**Multi-Level Bank Locker Security System Using Raspberry Pi with Face, Fingerprint, and OTP Verification** The objective is to create a Raspberry Pi–based multi-level bank locker system using face recognition, fingerprint scanning, and OTP verification to enhance security and prevent unauthorized access. .	**Embedded**
49.	TEMBMA3768	**AI-Powered Receptionist Robot with Facial Recognition and Voice Interaction**	

		The objective is to design a Raspberry Pi–based bank locker system with face recognition, fingerprint scanning, and OTP verification, ensuring multi-level security and protection of valuable assets.	**Robotics**
50.	**TEMBMA3769**	**IoT-Based Real-Time Crop Irrigation, Disease Identification, and Animal Intrusion Alert System** The objective is to create an IoT-based smart farming system that automates irrigation, identifies crop diseases, and detects animal intrusions in real time, ensuring water efficiency, crop protection, and improved productivity.	**IOT**
51.	**TEMBMA3770**	**Detect driver drowsiness in real time using eye tracking sensors, and send alert messages to nearby vehicles using VANET, improving road safety and reducing accidents** The objective is to develop a real-time drowsiness detection system using eye tracking sensors that sends alerts via VANET to nearby vehicles, improving road safety and reducing accident risks.	
52.	**TEMBMA3771**	**Design of an Edge-AI Embedded System for Underground Water Quality Surveillance** The objective is to design an edge-AI embedded system that monitors underground water quality in real time, enabling early contamination detection and promoting safe, sustainable water management.	**AI**
53.	**TEMBMA3772**	**Al-Powered Yield Estimation System using On-Field Image Data and Soil Parameters** The objective is to build an AI-based system that analyzes crop images and soil parameters to accurately estimate yield, helping farmers optimize resources and boost productivity.	**AI**
54.	**TEMBMA3773**	**Edge AI-Enabled Smart Vision Assistant for Visually Challenged Individuals** The objective is to develop a portable edge-AI system that recognizes objects, text, and surroundings in real time, offering	**Deep Learning**

		voice-based assistance to enhance independence and safety for visually impaired individuals.	
55.	TEMBMA3774	**FitMat AI: Smart Yoga Mat for Personalized Wellness Journey** The objective is to develop an AI-powered smart yoga mat that tracks postures, provides real-time feedback, and delivers personalized guidance to enhance practice, wellness, and healthy living.	**Machine Learning**
56.	TEMBMA3775	**AI-Powered Fracture Detection in Medical Images Using Hybrid Learning Architectures** The objective of this project is to build an AI-based system using hybrid learning to accurately detect bone fractures from medical images, ensuring faster and more reliable diagnosis for improved patient care.	**Machine Learning**
57.	TEMBMA3776	**Embedded-Based Real-Time Assistance and Safety System for Alzheimer's Patients** The objective is to build an embedded system that offers real-time monitoring, tracking, and emergency alerts to ensure safety and provide assistance for Alzheimer's patients.	**Embedded**
58.	TEMBMA3777	**Railway Safety Robot for Real-Time Track Error Detection Using GPS** The objective is to design a railway safety robot that uses GPS to detect track errors or damages in real time, ensuring timely maintenance and improved railway safety.	**Robotics**
59.	TEMBMA3778	**AI-Driven Disaster Forecasting and Response System Using Neural Networks** The objective is to build an AI-based system using neural networks to accurately predict natural disasters and provide timely alerts with response strategies, reducing risks and improving disaster management.	**Machine Learning**
60.	TEMBMA3779	**AI Enabled fire extinguisher robot with thermal Camera detection and Alert System**	**Robotics**

		The objective is to develop an AI-powered fire extinguisher robot with a thermal camera that detects fires in real time, extinguishes them, and sends instant alerts for faster response and enhanced safety.	
61.	**TEMBMA3780**	**AI Powered Number plate recognition with Automatic Toll Payment** The objective is to develop an AI-driven system that recognizes vehicle number plates and automates toll payments, ensuring faster transactions, reduced traffic congestion, and improved transportation efficiency.	**Machine Learning**
62.	**TEMBMA3781**	**Lightweight and Secure Framework for Medical Image Querying at the Edge** The objective is to create a secure and efficient edge-based system for storing and querying medical images, ensuring privacy and faster medical decision-making.	
63.	**TEMBMA3782**	**Intelligent Vertical Garden for Indoor Air Quality Monitoring Using IoT** The objective is to create an AI bot that monitors exam halls in real time, detects suspicious movements and sounds, and sends instant alerts to invigilators to prevent malpractice and ensure exam fairness.	**IOT**
64.	**TEMBMA3783**	**AI-Enhanced Skin Cancer Screening with CNN on Edge Devices using Raspberry Pi** The objective is to develop a lightweight, real-time Raspberry Pi system using CNNs to detect skin cancer from images, enabling early diagnosis, affordable screening, and accessible healthcare.	**Machine Learning**
65.	**TEMBMA3784**	**An Innovative Smart Irrigation Using Embedded and Regression-Based Machine Learning Technologies for Improving Water Security and Sustainability**	**Machine Learning**

		The objective is to develop a smart irrigation system using embedded devices and regression-based ML to optimize water use, improve crop growth, and ensure sustainable agriculture.	
66.	**TEMBMA3785**	**Edge AI-Powered Food Calorie Estimation for Real-Time Dietary Assessment on Raspberry Pi** The objective is to develop an edge AI system on Raspberry Pi that estimates food calories in real time, enabling effective diet tracking and healthier lifestyle management.	**Machine Learning**
67.	**TEMBMA3786**	**IoT-Enabled Autonomous Wheelchair with Real-Time Health Monitoring and Intelligent Navigation Assistance** The objective is to create an IoT-enabled smart wheelchair that offers real-time health monitoring and autonomous navigation, improving safety, mobility, and independence for users.	**IOT**
68.	**TEMBMA3787**	**Real-Time Safety Helmet Detection on Construction Sites Using YOLO Models and Raspberry Pi** The objective is to create a real-time vision-based system using YOLO and Raspberry Pi to detect helmet usage on construction sites, improving workplace safety and preventing accidents.	**Machine Learning**
69.	**TEMBMA3788**	**Smart Stick to Detect wildlife Animals for Trekkers Using Raspberry Pi** The objective is to develop a portable Raspberry Pi–based smart stick that detects nearby wildlife and provides real-time alerts to ensure trekkers' safety during outdoor activities.	**Machine Learning**
70.	**TEMBMA3789**	**Raspberry Pi-Based Non-Invasive Anemia Detection via Palpebral Conjunctiva Image Analysis** The objective of Raspberry Pi-Based Non-Invasive Anemia Detection via Palpebral Conjunctiva Image Analysis is to develop a low-cost system that analyzes eye images to detect anemia without blood tests. This enables quick, portable, and non-invasive health screening.	**Image Processing**
71.	**TEMBMA3790**	**AI-Based Intelligent Garbage Classification and Disposal System**	**Machine Learning**

		The objective is to develop an AI-based system that classifies and disposes of waste into categories such as biodegradable, recyclable, and hazardous, promoting recycling and sustainable waste management.	
72.	TEMBMA3791	**Renal Care: Personalized Alerting System for Renal Cancer Recurrence Prevention via IoT and ML** The objective is to develop an IoT- and ML-based system that monitors patient data, predicts renal cancer recurrence risks, and sends personalized alerts for timely intervention.	**IOT+ Machine Learning**
73.	TEMBMA3792	**Coin Operated Water ATM with Bottle Dispenser** The objective of Coin Operated Water ATM with Bottle Dispenser is to design an automated system that dispenses purified water and bottles upon coin insertion. It provides an affordable, user-friendly, and efficient solution for clean drinking water access.	**Embedded**
74.	TEMBMA3795	**Design and Implementation of a Cloud-Based Water Environment Monitoring System Using Internet of Things** The main objective is to monitor and maintain water quality in real time for environmental safety and sustainable management. This is achieved using sensors (pH, turbidity, temperature, dissolved oxygen) connected to an ESP32 microcontroller, transmitting data via Wi-Fi/GSM to a cloud platform for remote monitoring and analysis.	**IOT**
75.	TEMBMA3796	**Development of a Wireless Communication System for Automated Devices** The main objective is to develop a wireless communication system that allows automated devices to operate and communicate without manual intervention. This system uses microcontrollers, wireless modules, and sensors/actuators to enable remote monitoring, control, and efficient automation of devices.	**WSN**
76.	TEMBMA3797	**Design of a Portable Heart Rate and Temperature Monitoring System for the Elderly**	**Biomedical**

		The main objective is to design a portable system that continuously monitors heart rate and body temperature of elderly individuals. The system uses sensors and a microcontroller to collect real-time data and provides alerts for abnormal readings to ensure timely medical attention and better health management.	
77.	TEMBMA3798	**Design and Implementation of Aquaculture Farm Environment Monitoring System Based on IoT** The main objective is to design and implement an IoT-based system that monitors key environmental parameters of an aquaculture farm, such as water temperature, pH, and dissolved oxygen. The system collects real-time data using sensors and a microcontroller, uploads it to the cloud, and enables remote monitoring and management to ensure optimal conditions for aquatic life.	**IOT**
78.	TEMBMA3799	**Tomato planting environment monitoring and pest warning system based on Internet of Things and Huawei ModelArts** The main objective is to develop an IoT-based system that monitors the tomato planting environment, including temperature, humidity, soil moisture, and light conditions. Using sensors, microcontrollers, and Huawei ModelArts for data analysis, the system provides real-time monitoring and pest warnings to help farmers maintain healthy crops and improve yield.	**OpenCV**
79.	TEMBMA3800	**Weather Monitoring for Curating Cricket Pitches using Machine Learning and Arduino** The main objective is to monitor and maintain ideal cricket pitch conditions by measuring weather and soil parameters using sensors and Arduino. It aims to collect real-time data on temperature, humidity, soil moisture, and sunlight. This data is then used to guide pitch curation decisions for consistent playing quality.	**Machine learning**
80.	TEMBMA3801	**Unlocking Water Conservation: Synergizing IoT and Machine Learning for Agricultural Irrigation Efficiency** The main objective is to optimize agricultural irrigation by monitoring soil and environmental conditions using IoT sensors	**Machine learning**

		and Arduino. The system uses real-time data and machine learning to ensure crops receive optimal water while conserving water resources.	
81.	TEMBMA3802	**A Mobile Unit for Weather Monitoring and Prediction Using IoT and Machine Learning** The main objective is to implement a mobile unit equipped with IoT sensors that collects real-time environmental data. This data is processed using machine learning algorithms to predict weather conditions and provide timely alerts.	**IOT**
82.	TEMBMA3803	**Arduino Based Secured Access Control in Smart Homes by Implementing Anomaly Detection in Fingerprint - Based Door Lock and Realtime Monitoring with OpenCV** The main objective is to secure smart homes by implementing a fingerprint-based door lock system with anomaly detection. The project is done by using an Arduino to control the door lock, integrating a fingerprint sensor for authentication, and employing OpenCV for real-time monitoring and detection of unauthorized access attempts.	**Embedded Applications**
83.	TEMBMA3804	**IoT-Based Smart Biofloc Monitoring System for Fish Farming Using Machine Learning** The main objective is to monitor and maintain optimal conditions in biofloc fish farming using IoT sensors and machine learning. The system uses sensors like pH, temperature, dissolved oxygen, and turbidity to collect real-time water quality data, which is analyzed to ensure healthy fish growth and automate alerts for abnormal conditions. .	**Machine learning**
84.	TEMBMA3805	**Hand Gesture Control Robo Car using Machine Learning** The main objective is to control a robotic car using hand gestures recognized through machine learning. The project is done by using a camera to capture hand movements, an Arduino or microcontroller to control the motors via an L298N motor driver, and a trained machine learning model to interpret gestures and move the car accordingly.	**Robotics**
85.	TEMBMA3806	**Zigbee Based Real Time Earthquake Monitoring and Alert System Using IoT**	**WSN**

		The main objective is to detect earthquakes in real-time and provide immediate alerts using IoT and Zigbee communication. The project is done by using vibration or accelerometer sensors to sense seismic activity, Arduino for data processing, and Zigbee modules to transmit alerts to monitoring stations or mobile devices instantly.	
86.	**TEMBMA3807**	**LoRa Video Streaming in Rural Wireless Multimedia Sensor Networks** The main objective is to implement long-range, low-power video streaming in rural areas using LoRa-based wireless multimedia sensor networks. The project is done by using cameras with LoRa transceivers to capture and transmit video data, microcontrollers for processing, and a central receiver unit to collect and display the video in real-time, enabling monitoring in areas with limited connectivity.	**WSN**
87.	**TEMBMA3808**	**Early Prediction of Heart Diseases Using Machine Learning Algorithms-A Review** The main objective is to predict the risk of heart diseases early using machine learning algorithms. The project is done by collecting patient health data (like blood pressure, cholesterol, ECG readings) through sensors or medical records, processing it with machine learning models, and generating predictions to help in timely diagnosis and preventive care.	**Machine learning**
88.	**TEMBMA3809**	**Letter and Person Recognition in Freeform Air-Writing Using Machine Learning Algorithms** The main objective is to recognize letters and identify individuals from freeform air-writing using machine learning. This is achieved by capturing hand movements with a camera or motion sensor, processing the data with ML algorithms to interpret the letters, and analyzing writing patterns for person recognition.	**Machine learning**

89.	TEMBMA3815ss	**Edge Computing Application-Specific Integrated Circuit With Two Serial Communication Protocols and a Backpropagation Neural Network** The main objective is to implement an edge computing system entirely using embedded systems, integrating two serial communication protocols with a backpropagation neural network. The system processes sensor data locally on the embedded hardware, enabling real-time intelligent decision-making without external computing resources.	**Embedded Applications**
90.	TEMBMA3811	**Autonomous Fire Extinguisher Rover with Self-Preservation and Emergency Protocols Using Arduino** The main objective is to develop an autonomous fire-extinguisher rover that detects and extinguishes fires while following self-preservation and emergency protocols. The project is done using Arduino, flame and temperature sensors for fire detection, motors and motor drivers for movement, and a water pump or extinguisher mechanism to suppress fires automatically.	**Arduino**
91.	TEMBMA3812	**Private Cloud Storage using Raspberry PI via Virtual Network Computing - An Analysis** The main objective is to implement a private cloud storage system using Raspberry Pi with secure remote access via Virtual Network Computing (VNC). This is done by configuring the Raspberry Pi as a cloud server, connecting external or internal storage for hosting data, setting up network and user authentication, and using VNC to enable real-time file access, upload, and management from remote devices while ensuring security and reliability.	**OpenCV**
92.	TEMBMA3813	**Affordable Smart ECG Monitoring Using Arduino & Bluetooth Module** The main objective is to provide an affordable system for real-time ECG monitoring using Arduino and Bluetooth. The project is done by using an ECG sensor to capture heart signals, Arduino to process the data, and a Bluetooth module to transmit the readings to a smartphone or computer for display and analysis.	**Embedded Applications**

93.	TEMBMA3814	**Raspberry Pi Based Vehicle Collision Avoidance System** The main objective is to prevent vehicle collisions using a Raspberry Pi-based real-time monitoring system. The project is done by using ultrasonic sensors to detect obstacles, a Raspberry Pi to process sensor data and make decisions, and actuators or alerts to warn the driver or automatically control the vehicle to avoid collisions.	**OpenCV**
94.	TEMBMA3818	**Head Motion Controlled Wheel Chair** The main objective of this project is to develop a Head Motion Controlled Wheelchair that enables physically challenged individuals to control movement using head gestures. It aims to ensure safe, smooth, and reliable navigation by interfacing motion sensors with a microcontroller. The project also focuses on creating a low-cost prototype that promotes user independence and comfort.	**Biomedical Applications**
95.	TEMBMA3819	**ESP32-Based Smart Fan with Energy Monitoring and Scheduling via Android App** The main objective of this project is to develop an ESP32-Based Smart Fan with Energy Monitoring and Scheduling via Android App that enables users to remotely control and monitor fan operation. It tracks real-time energy usage and optimizes power consumption through automated scheduling. The project focuses on creating a prototype that demonstrates efficient, convenient, and energy-saving smart control using IoT technology.	**IoT**
96.	TEMBMA3820	**ESP32-Based Smart Power Factor Correction and Load Balancing** The main objective of this project is to develop an ESP32-Based Smart Power Factor Correction and Load Balancing System that enhances electrical efficiency by monitoring and automatically correcting the power factor in real time. It intelligently balances connected loads to reduce energy losses and prevent overloading. The project focuses on creating a prototype that demonstrates real-time monitoring, automatic correction, and smart power management using IoT technology.	**Embedded Applications**

97.	TEMBMA3821	**IoT-Based Atmospheric Pollution Level Analyzer using Raspberry Pi** The main objective of this project is to develop an IoT-Based Atmospheric Pollution Level Analyzer using Raspberry Pi that monitors air quality in real time using environmental sensors. It detects harmful gases and particulate matter, uploading data to an IoT platform for remote monitoring and alerts. The project focuses on creating a prototype that ensures accurate sensing, data logging, and cloud-based visualization of pollution levels.	**IoT**
98.	TEMBMA3822	**ESP32-Based Smart Air Purifier with Real-Time Pollution Data Upload** The main objective of this project is to develop an ESP32-Based Smart Air Purifier with Real-Time Pollution Data Upload that monitors air quality using sensors and automatically adjusts the purifier's operation based on pollution levels. It uses the ESP32 for real-time control and IoT connectivity to upload data to the cloud. The project focuses on creating a prototype that ensures intelligent air purification, energy efficiency, and remote monitoring.	**IoT**
99.	TEMBMA3823	**AI-Driven Crop Growth Prediction using Raspberry Pi** The main objective of this project is to develop an AI-Driven Crop Growth Prediction System using Raspberry Pi that uses sensors to monitor environmental parameters and predict crop growth through machine learning. It helps farmers make accurate decisions for better yield. The project focuses on creating a prototype that enables intelligent prediction and real-time monitoring for smart farming.	**Machine Learning**
100	TEMBMA3824	**Raspberry Pi-Based Carbon Footprint Analyzer for Smart Homes** The main objective of this project is to develop a Raspberry Pi-Based Carbon Footprint Analyzer for Smart Homes that monitors household energy usage and calculates real-time carbon emissions. It processes sensor data to display results through the Raspberry Pi. The project focuses on building a	**Opencv**

		prototype that encourages energy efficiency and sustainable living through smart monitoring.	
101	TEMBMA3825	**ESP32-Based Smart Gas Leak and Explosion Predictor** The main objective of this project is to develop an ESP32-Based Smart Gas Leak and Explosion Predictor that detects gas leaks and predicts potential hazards in real time. It uses the ESP32 for processing and IoT alerts to ensure safety. The project focuses on building a prototype that provides accurate detection, early warnings, and effective prevention of gas-related accidents.	**IoT**
102	TEMBMA3826	**IOT BASED INPLANATBLE AI PILL (Tablet) DEVELOPMENT FOR MEDICINE TRACKING** The main objective of this project is to develop an IoT-Based Implantable AI Pill (Tablet) for Medicine Tracking that monitors the pill's position, temperature, and pH levels in real time. It uses sensors and wireless communication for AI-based analysis of medicine intake. The project focuses on building a prototype that improves medication tracking and patient care through smart health monitoring.	**IoT**
103	TEMBMA3832	**Design and Implementation of Intelligent Dressing Mirror Based on Raspberry Pi 4B** The objective of this project is to develop an intelligent dressing mirror using Raspberry Pi 4B that enhances personalized smart-home experiences through cloud connectivity and real-time sensing. The system integrates Alibaba Cloud's MQTT service for managing clothing data and uses onboard sensors and cameras to collect environmental and user information. By analyzing these inputs, the mirror provides context-aware outfit recommendations along with essential updates such as weather, date, and schedules, offering a low-power, convenient, and personalized home-automation solution.	**Machine Learning / IoT**

104	TEMBMA3833	**Google pi using raspberry pi for visually impaired** The objective of this project is to develop Google Pi, a voice-assisted system using Raspberry Pi that enhances the independence and safety of visually impaired users. The system integrates Google's voice assistant API with deep learning algorithms to provide real-time object and currency recognition, enabling users to identify their surroundings and manage financial tasks autonomously. By combining voice interaction with intelligent visual recognition, Google Pi aims to improve accessibility, facilitate efficient daily activities, and promote a safer, more independent lifestyle for visually challenged individuals.	**Deep Learning / Assistive Technology1**
105	TEMBMA3834	**Raspberry Pi: AWS Automated Smart Greenhouse:**The objective of this project is to develop an automated smart greenhouse using Raspberry Pi 4 that monitors temperature and humidity to control a heater and fan, maintaining optimal conditions. The system also provides a dashboard for real-time environmental data and device status, offering a low-cost, reliable, and scalable solution for precise climate management.	**IoT / Automation**
106	TEMBMA3835	**Raspberry-Pi-based Pick and Place Robotic Arm for the Chemical Industry** The objective of this project is to develop a Raspberry-Pi-based robotic arm to safely handle hazardous chemicals in the chemical industry. The system automates container transfer with 360-degree movement, controlled via Python, and integrates IoT for real-time monitoring and remote access, ensuring efficiency and safety.	**Robotics / IoT**
107	TEMBMA3836	**Cardiovascular Disease Diagnosing Using Machine Learning** The objective of this project is to develop an Arduino-based heart monitoring system that uses sensors and machine learning (Bagging algorithm) to provide real-time cardiac health insights. The system aims to enable continuous, remote monitoring with alerts for abnormal readings, improving early detection, accessibility, and proactive management of cardiovascular diseases.	**Machine Learning / Healthcare**

108	TEMBMA3837	**Next-Generation IoT Smart Cradle System for Infant Health and Monitoring** The objective of this project is to develop an IoT-based smart cradle that monitors a baby's movements and nursery conditions, automatically rocks the baby, and streams live audio-video to caregivers. The system aims to enhance infant safety, enable remote monitoring, and provide real-time alerts while ensuring data security and privacy.	**IoT / Embedded Systems**
109	TEMBMA3838	**Rethinking 3-D LiDAR Point Cloud Segmentation** The objective of this project is to improve the efficiency and accuracy of 3-D LiDAR point cloud segmentation by reformulating point-based operations to work in projection space. The system aims to integrate these operations into a 2-D encoder-decoder architecture, combining the advantages of point-based and image-based methods to achieve faster, more robust, and accurate semantic segmentation in outdoor environments.	**Deep Learning / Computer Vision**
110	TEMBMA3839	**Brain Tumor Identification and Classification of MRI Images Using Deep Learning Techniques:** The objective of this project is to develop a fully automatic deep learning-based system for brain tumor detection and segmentation from MRI images. The system aims to accurately identify abnormal and normal brain tissues using FAHS-SVM and probabilistic neural networks, improving diagnostic efficiency, reducing reliance on manual analysis, and achieving high accuracy in medical imaging.	**Deep Learning / Medical Imaging**
111		**RFID which detects the icons beside the road Automatic speed regulation of vehicles based on speed zones using RF technology:** The objective of this project is to develop an RFID-based smart vehicle system that alerts drivers about upcoming road zones and speed limits, providing visual and audio warnings in real time. The system aims to automatically monitor and control vehicle speed according to zone restrictions, enhancing road safety, reducing accidents, and providing a more efficient alternative to static road signs.	**Embedded Systems**

112		**IOT based Anti-theft Flooring System using Raspberry Pi:** The objective of this project is to develop an IoT-based anti-theft floor mat system using Raspberry Pi that monitors floor movements and provides real-time alerts and surveillance. The system aims to enhance home security by enabling remote monitoring, capturing intruder activity via sensors and camera, and ensuring data privacy, scalability, and rapid response to unauthorized access.	**IoT / Security**
113	**TEMBMA3842**	**Integrating Edge AI and IoT: A Deep Learning Approach to Safe Guard Crops from Wildlife Threats:** The objective of this project is to develop a real-time, scalable Edge AI and IoT system for detecting, classifying, and deterring animal intrusions in farms. Using laser perimeters, cameras, and the YOLOv8m model on Raspberry Pi with Hailo-8 AI Accelerator, the system aims to provide accurate intrusion detection, immediate alerts, and effective deterrence while ensuring low-latency processing, data privacy, and improved crop protection.	**Edge AI / IoT / Agriculture**
114	**TEMBMA3843**	**ZIGBEE or RF and internet based advanced street light controlling system:** The objective of this project is to design and implement an advanced street light control system using ZigBee communication that overcomes the limitations of existing systems. It aims to provide easy handling, simplified maintenance, and economical operation of complex street lighting networks, ensuring efficient and reliable urban lighting management.	**IoT / Smart City**
115	**TEMBMA3844**	**Real-Time Mushroom Detection and Maturity Classification Using YOLO-Tiny on Raspberry Pi Platform:** The objective of this project is to develop a real-time mushroom detection and maturity classification system using YOLOv3-tiny and YOLOv4-tiny on low-power embedded devices, enabling automated monitoring, improved harvesting efficiency, and enhanced operational productivity in mushroom farming.	**Computer Vision / Smart Farming**

116	TEMBMA3846	**A ZigBee-Based Healthcare Monitoring System** The objective of this project is to develop an intelligent ZigBee-based healthcare monitoring system for elderly individuals that continuously tracks vital signs and environmental risks, detects falls or abnormal conditions using machine learning, and provides real-time alerts and remote access via Raspberry Pi and cloud integration, enhancing safety, health monitoring, and caregiver support in smart homes.	**IoT / Healthcare**
117	TEMBMA3847	**AI-Driven Child Safety System: Real-Time Fear Detection and Emergency Response using Enhanced Deep Learning Algorithms:** The objective of this project is to develop an AI-powered child safety system that monitors children in real time, detects fear or distress using CNN and KNN models, and provides immediate alerts, environmental data, and emergency guidance to parents and authorities, enabling faster intervention and enhanced protection in critical situations.	**AI / Child Safety**
118	TEMBMA3848	**Design of a Raspberry Pi 4B-Based Guide Robot with YOLO-v10 Integration:** The objective of this project is to design an intelligent guide robot using Raspberry Pi 4B and YOLO-v10 that assists visually impaired individuals in safe navigation by detecting obstacles, providing real-time voice-guided directions, and enabling remote monitoring for enhanced safety and independence.	**Robotics / Assistive Technology**
119	TEMBMA3850	**Real-Time Tray-Level Egg Fertility Detection on Raspberry Pi Using YOLOv5 and Custom LED Backlighting:** The objective of this project is to develop a low-cost, portable, and automated egg fertility scanner using Raspberry Pi 4B and YOLOv5 to accurately detect and classify fertile and infertile eggs in real-time, reducing manual labor, processing time, and human error in hatchery operations.	**Machine learning**

120	TEMBMA3851	**SolarSync - Smart Sun Tracking Technology** The primary objective of this project is to design and develop an adaptive driver drowsiness detection system based on the Eye Characteristic Ratio (ECR) to continuously monitor a driver's eye behavior in real time. The system aims to accurately identify signs of drowsiness by analyzing eye closure, blinking patterns, and fatigue-related variations under different lighting and driving conditions. By providing timely alerts and warnings to the driver, the proposed approach seeks to reduce fatigue-related accidents and enhance overall road safety.	**Ai**
121	TEMBMA3852	The main objective of this project is to design and implement a sustainable water management system for tomato cultivation using an evolving testbed approach. The system aims to optimize water usage by continuously monitoring soil moisture and environmental conditions, adapting irrigation strategies to the changing growth stages of tomato plants. By reducing water wastage, improving crop health, and enhancing yield efficiency, the proposed model supports sustainable agriculture and promotes efficient resource utilization in modern farming practices.	**Embedded**
122	TEMBMA3853	**Urban Agriculture through IoT-Based Resilient Hydroponic Farming — A Machine Learning Approach** The objective is to design an IoT-based hydroponic farming system for urban agriculture that uses machine learning to monitor, predict, and optimize plant growth conditions. The system aims to improve crop yield, resource efficiency, and sustainability by intelligently controlling environmental and nutrient parameters.	**IOT**
123	TEMBMA3854	To design and implement energy-efficient Green AI–based predictive models for smart agriculture that accurately forecast crop yield and optimize resource management (water, energy, fertilizers) by minimizing computational power consumption while maintaining high prediction accuracy, thereby promoting sustainable and eco-friendly farming practices.	**Ai**

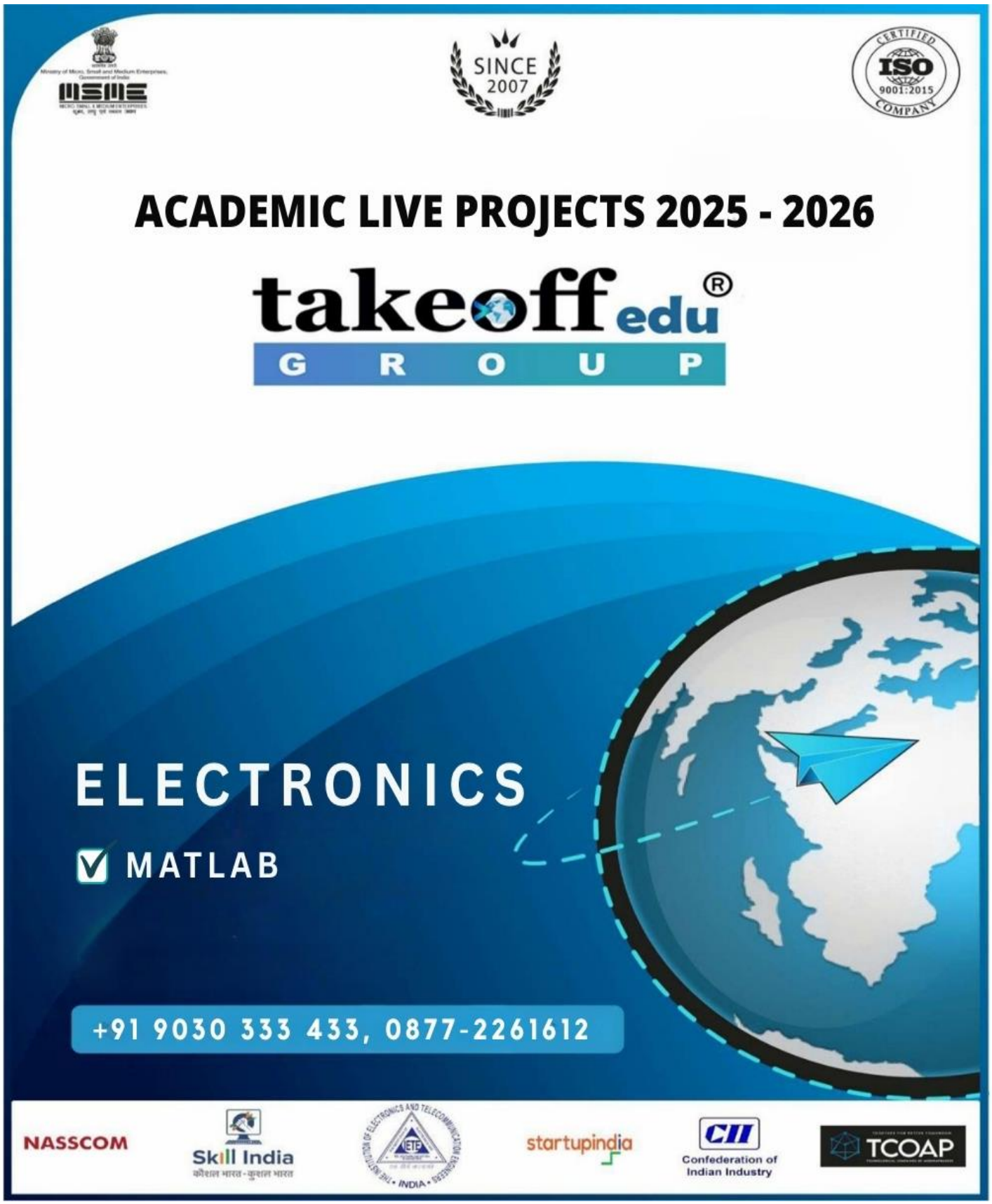
124	TEMBMA3855	**Automated SMS-Based Vaccination Reminder System for Child Health Management** To design and implement an automated system that sends timely SMS alerts to parents or guardians reminding them about their children's upcoming and missed vaccination schedules, thereby improving immunization compliance, reducing dropouts, and ensuring better child health management.	**Iot**
125	TEMBMA3855	**Children vaccination reminder via SMS alert** The main objective of the Child Safety and Activity Monitoring System Using IoT is to design and develop a smart, real-time monitoring system that ensures child safety by continuously tracking the child's location, activity patterns, and environmental conditions using IoT-enabled sensors. The system aims to alert parents or guardians instantly in case of abnormal activity, unsafe movement, or emergency situations, thereby improving supervision, response time, and overall child security.	**Iot**
126	TEMBMA3857	**Automated Ration Vending using RFID** The main objective of the Automated Ration Vending Using RFID system is to automate and secure the public distribution of ration commodities by using RFID technology. This system aims to reduce manual intervention, eliminate corruption and fraud, ensure accurate quantity distribution, maintain transparency in ration delivery, and provide faster, reliable service to beneficiaries through authentication using RFID cards.	**Embedded**
127	TEMBMA3858	**Intelligent Gesture-based Robotic System with MEMS and RF Technology for Enhanced Motion Control using ESP32 CAM** The objective of the Intelligent Gesture-based Robotic System with MEMS and RF Technology using ESP32-CAM is to design and develop a smart robotic control system that interprets human hand gestures using a MEMS sensor and wirelessly transmits control commands through RF communication. The system aims to achieve precise, real-time motion control of a robotic platform while enhancing user interaction, flexibility, and safety. The integration of the ESP32-CAM enables visual monitoring, making the system suitable for remote operation,	**Embedded**

		surveillance, and assistive robotic applications with improved accuracy and responsiveness.	
128	TEMBMA3859	**Web-based online embedded door access control and home security system based on face recognition** To design and implement a web-based embedded door access control and home security system that uses face recognition to authenticate users, allowing only authorized individuals to access the premises while enabling real-time monitoring, access logging, and remote control through an online web interface for enhanced home security and convenience.	**Iot**
129	TEMBMA3860	**Enhanced Intelligent Attendance Management System for Smart Campus Using Computer Vision** The main objective of this project is to design and develop an automated attendance management system for a smart campus using computer vision techniques. The system aims to accurately identify and recognize individuals through facial recognition, automatically record attendance in real time, reduce manual effort and human errors, prevent proxy attendance, and improve efficiency, security, and data management within educational institutions.	**Ai**
130	TEMBMA3861	**Monitoring Home Security by Developing an IoT-Based Smart Home Automation System Controlled by Android App and Web** To design and develop an IoT-based smart home automation and security monitoring system that allows users to remotely control home appliances and monitor security conditions in real time through an Android application and a web-based interface, thereby improving safety, convenience, and energy efficiency.	**Iot**
131	TEMBMA3862	**Design of Car Anti-theft System Based on Face Recognition** The main objective of this project is to design and develop an intelligent car anti-theft system that uses face recognition technology to allow vehicle access only to authorized users. The system aims to enhance vehicle security by automatically identifying the driver's face, preventing unauthorized access, reducing theft incidents, and improving safety through real-time authentication and alert mechanisms.	**iot**

132	TEMBMA3864	**Airbag System for Elderly People Fall Protection with Proactive Safety Measures** The objective of this project is to design a wearable airbag system that protects elderly people from injuries caused by falls. The system aims to detect falls using sensors connected to a microcontroller. It automatically deploys an airbag to reduce impact during a fall. The system also monitors basic health parameters such as heart rate, body temperature, and force. Additionally, it sends alert notifications wirelessly to a mobile application for timely assistance.	**Iot /health care**
133	TEMBMA3866	**SmartLib: Automated Library Management with RFID and Mobile Alerts** The objective of this project is to develop an Automated Library Management System that simplifies and improves library operations. The system aims to reduce manual work and minimize errors in maintaining records. It uses Arduino, RFID technology, and an LCD display for efficient data handling. The BLYNK software helps in monitoring member details, book status, and updates in real time. Overall, the system saves time, reduces cost, and makes library management more user-friendly.	**Iot**
134	TEMBMA3869	**Computational Intelligence and IoT in Transforming Agricultural Environmental Control** This study explores the integration of computational intelligence and Internet of Things (IoT) technologies in transforming agricultural environmental control systems. IoT-based sensors continuously monitor critical parameters such as temperature, humidity, soil moisture, and light intensity. Computational intelligence techniques analyze the collected data to enable predictive decision-making and automated control. The proposed approach enhances crop productivity, resource efficiency, and sustainable agricultural practices.	**iot**

135	TEMBMA3870	**TinyML-Enabled Resource-Efficient Framework for Real-Time Network Securiy in Electric Vehicle Charging Networks** This work proposes a TinyML-enabled, resource-efficient framework for ensuring real-time network security in electric vehicle charging networks. The system deploys lightweight machine learning models on edge devices to detect anomalies and potential cyberattacks with minimal computational overhead. By processing data locally, the framework reduces latency and dependence on cloud resources. The proposed solution enhances the security, reliability, and scalability of EV charging infrastructure.	**AI**
136	TEMBMA3871	**Real-Time Hand Gesture Recognition for LED Control using CNN and Arduino** This project presents a real-time hand gesture recognition system for controlling LEDs using a Convolutional Neural Network (CNN) and Arduino. The system captures hand gestures through a camera and processes them using a trained CNN model for gesture classification. Recognized gestures are sent to an Arduino microcontroller to control LED operations in real time. The proposed approach offers an intuitive, touchless, and efficient human–machine interaction system.	**AI**
137	TEMBMA3872	**An IoT Based Assessment in Workspaces: Indoor Air Quality vs Thermal Comfort** This study presents an IoT-based system for assessing indoor air quality and thermal comfort in workspaces such as educational institutions and hospitals. The system monitors key air pollutants including CO_2, PM2.5, and TVOCs, along with temperature and humidity, using a custom-built sensor network. Real-time data is processed through complex event processing and analyzed using machine and deep learning techniques. An LSTM model forecasts IAQ, while a decision tree regressor identifies relationships between environmental parameters and pollutants.	**Iot**

138	TEMBMA3868	**An Adaptive Fast-Response Sensor Integrated Smart Helmet for Blind-Spot Protection and Guidance to Avoid Unavoidable Occurrences** Motorcycles are increasing in numbers as more online travel services are becoming available, and it is easier and cost efficient for both the rider and driver to travel places in Bangladesh. As the number of motorcycles increases, so are the chances of accidents related to them. The idea behind developing this proposed model roots from the social responsibility we have towards society. The primary causes of death due to accidents are the lack thereof emergency medical services and information relating to the accident such time, place, and other factors. The aim of this proposed model design is to provide necessary services in the event of a motorcycle accident so that necessary actions can be taken to save the life of the injured and give blind-spot protection to the rider. This system is based on Arduino and consists of microcontrollers, GSM, GPS, and sensors for the detection of the accident and to examine the condition of the rider.	**Iot**
139	TEMBMA3873	**SolarSync - Smart Sun Tracking Technology** The objective of SolarSync – Smart Sun Tracking Technology is to develop an intelligent solar tracking system that continuously aligns solar panels with the sun's position to achieve maximum energy absorption. The system aims to reduce power losses associated with fixed solar panels by using real-time sensing and automated control mechanisms. By integrating smart sensors and efficient tracking algorithms, SolarSync enhances the overall efficiency, reliability, and performance of solar energy generation. Additionally, the project focuses on creating a cost-effective and scalable solution that can be deployed in both residential and industrial solar power applications.	**Deep learning**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LATEST MATLAB ACADEMIC LIVE PROJECTS 2025-2026

S. No	Project Code	Title	Domain
1.	TMMACO171	**Deep Reinforcement Learning-Driven Secure ISAC Optimization Using STAR-RIS in 6G Networks** **Objective:** To develop a DRL-based framework using Soft Actor-Critic for optimizing secure multi-user ISAC systems with STAR-RIS, enhancing 6G communication, sensing, and security performance.	Communication
2.	TMMACO172	**Secure THz Communication in 6G: A Two-Stage DRL Approach for IRS-Assisted NOMA** **Objective:** To optimize secrecy energy efficiency in IRS – assisted THz – NOMA systems using a two-stage DDPG-based deep reinforcement learning approach.	Communication
3.	TMMACO174	**Performance Enhancement of V2V Communication by QC-LDPC Code and NOMA-UM-MIMO Techniques** **Objective:** This project aims to enhance V2V communication reliability and capacity by integrating QC-LDPC coding, NOMA, and UM-MIMO under Rician fading using MATLAB-based performance evaluation.	Communication
4.	TMMAIP453	**AI-Synthesized Image Detection: Source Camera Fingerprinting to Discern the Authenticity of Digital Images** **Objective:** This study aims to detect AI-generated facial images by extracting deep features using ResNet-101 and classifying them with an SVM for reliable authenticity verification.	Image Processing/Artificial Intelligence
5.	TMMAIP446	**BorB: A Novel Image Segmentation Technique for Improving Plant Disease Classification with Deep Learning Models** **Objective:** To develop BorB, an image segmentation technique using RGB and Lab b-channels to enhance plant disease classification accuracy with deep learning for precision agriculture applications.	Image Processing/Artificial Intelligence
6.	TMMAAI382	**Early Diagnosis of Alzheimer's Disease Using Adaptive Neuro K-Means Clustering Technique** **Objective:** To develop an efficient diagnostic model for early Alzheimer's detection using AMSOM-FKM segmentation,	Image Processing/Artificial Intelligence

		GLCM feature extraction, PCA-based reduction, and multi-class classification of brain MRI images.	
7.	TMMASP216	**A Resource-Efficient Time-Domain-Based Algorithm to Estimate Respiration Rate from Single-Lead ECG Signal** **Objective:** To develop a computationally efficient time-domain MPD algorithm for accurate breath rate estimation from single-lead ECG signals, enabling real-time wearable respiratory monitoring.	**Signal Processing**
8.	TMMASP221	**A Deep and Interpretable Learning Approach for Long-Term ECG Clinical Noise Classification** **Objective:** The objective is to develop explainable deep learning models to classify clinical noise severity in long-term ECG recordings, improving diagnostic accuracy and enhancing clinician trust in AI-based decision support.	**Signal Processing**
9.	TMMASP222	**Efficient Nearly Piecewise Continuous Signal Basis Expansion by Precision Calculation** **Objective:** This study proposes an adaptive signal expansion method that accurately reconstructs nearly piecewise continuous 1D signals by segmenting and expanding smooth and large-gradient regions separately.	**Signal Processing**
10.	TMMACO159	**Enhancing Security and Privacy in 5G Device-to Device Communication: A Secure Gale-Shapley Algorithm Approach** **Objective** To develop a robust AI-driven security framework for D2D communication in 5G networks, enhancing performance and protecting user data through adaptive jamming, differential privacy, MPC, and lightweight encryption.	**Communication**
11.	TMMAIP445	**A Comparative Study of Image Processing Techniques for Javanese Ancient Manuscripts Enhancement** **Objective** To evaluate and compare multiple image enhancement techniques for improving the readability and structural clarity of degraded Javanese ancient manuscripts using MATLAB, aiding in digital preservation and cultural documentation.	**Image Processing/Artificial Intelligence**
12.	TMMAAI367	**Optimized Brain Tumor Detection: A Dual-Module Approach for MRI Image Enhancement and Tumor Classification**	**Image Processing/Artificial Intelligence**

		Objective: The proposed method enhances brain tumor detection by applying adaptive Wiener filtering for noise reduction, RBF neural networks for feature extraction, and SVM for classification, improving tumor diagnosis and treatment planning.	
13.	TMMACO146	**Bandwidth Allocation and Power Control Optimization for Multi-UAVs Enabled 6G Network** **Objective**: To develop an optimized algorithm for power control and bandwidth allocation in multi-UAV networks, enhancing energy efficiency and spectrum utilization.	**Communication**
14.	TMMAAI374	**Comparative Analysis of Fingerprint Authentication Using the Convolutional Neural Network (CNN) Method for Two Datasets** **Objective**: The objective of this study is to analyze and compare CNN architectures for fingerprint authentication, enhancing accuracy, efficiency, and biometric security.	**Image Processing/Artificial Intelligence**
15.	TMMAAI381	**Detection of Acute Lymphoblastic Leukemia Using a Novel Bone Marrow Image Segmentation** **Objective** To develop an automated system using image processing and ANFIS classification for accurate detection and classification of Acute Lymphoblastic Leukemia (ALL) from segmented bone marrow cell images.	**Image Processing/Artificial Intelligence**
16.	TMMACO161	**Car-to-Car Communication Using RF Cognitive Radio with VLC Common Control Channel** **Objective** To develop a hybrid car-to-car communication system integrating Cognitive Radio with a VLC-based Common Control Channel, enhancing spectrum efficiency, reducing RF congestion, and ensuring cost-effective, reliable vehicular network communication.	**Communication**
17.	TMMAWS144	**Optimized Cluster Routing Protocol with Energy-Sustainable Mechanisms for Wireless Sensor Networks** **Objective:** To develop and evaluate novel clustering algorithms—IMP-RES-EL and EE-SEP—that enhance energy efficiency and network longevity in both homogeneous and heterogeneous wireless sensor networks by optimizing data transmission and reducing energy dissipation.	**Communication**

18.	TMMASP213	**OCADN: Improving Accuracy in Multi-Class Arrhythmia Detection from ECG Signals with a Hyper parameter-Optimized CNN** **Objective:** To develop an optimized CNN-based model (OCADN) with advanced pre-processing and hyper parameter tuning for accurate and robust arrhythmia detection from ECG signals, outperforming traditional LSTM approaches in classification performance.	**Signal Processing**
19.	TMMASP215	**ENHANCING SPEECH FOR HEARING IMPAIRED AIDS THROUGH CNN** **Objective**: To develop a real-time CNN-based speech enhancement system for hearing aid users, using log power spectrum features to improve speech intelligibility and quality while ensuring low latency on smartphones.	**Signal Processing**
20.	TMMACO138	**Millimeter-Wave Massive MU-MIMO Performance Analysis for Private Underground Mine Communications** **10Objective**: This article evaluates mmWave massive MU-MIMO channel characteristics in an underground mine, emphasizing path loss, time dispersion, and spectral efficiency.	**Communication**
21.	TMMAIP438	**Single Underwater Image Restoration Using Variational Framework Guided by Imaging Model with Noise** **Objective**: The objective is to enhance underwater image quality by integrating an improved imaging model with noise and variational frameworks for superior contrast, color correction, and noise suppression.	**Image Processing**
22.	TMMASP197	**Lightweight and High Accurate RR Interval Compensation for Signals from Wearable ECG Sensors** **Objective**: The objective is to develop a lightweight, high-accuracy RRI compensation method for wearable ECG sensors, balancing power consumption and resolution.	**Signal Processing**
23.	TMMASP194	**A Novel ECG Signal Quality Index Method Based on Skewness-MODWT Analysis.** **Objective**: Develop a novel Signal Quality Index (SQI) method to classify and optimize ECG signals for wearable devices, enhancing accuracy and efficiency.	**Signal Processing**

24.	TMMASP201	**A Morphology-Preserving Algorithm for Denoising of EMG-Contaminated ECG Signals** **Objective**: Develop a novel iterative regeneration method to efficiently suppress EMG noise in ECG signals, preserving diagnostic information.	**Signal Processing**
25.	TMMAIP440	**Online Low-Light Sand-Dust Video Enhancement Using Adaptive Dynamic Brightness Correction and a Rolling Guidance Filter** **Objective**: To enhance low-light sand-dust videos, an adaptive dynamic brightness correction and rolling guidance filter improve contrast, illumination, and noise reduction.	**Image Processing, Image Enhancement**
26.	TMMAAI332	**Lumbar Disease Classification Using an Involutional Neural Based VGG Nets (INVGG)** **Objective**: The objective is to classify lumbar diseases accurately using an advanced INVGG network that combines involutional layers with a modified VGG structure, enhancing diagnostic precision in medical imaging.	**Image Processing/Artificial Intelligence**
27.	TMMAWS94	**Wireless Sensor Network (WSN) Model Targeting Energy Efficient Wireless Sensor Networks Node Coverage** **Objective**: Designing and improving energy-efficient coverage methods for wireless sensor networks using the improved gray wolf algorithm to optimize node deployment.	**Communication**
28.	TMMAAI321	**Tomato Quality Classification Based on Transfer Learning Feature Extraction and Machine Learning Algorithm Classifiers** **Objective**: The study introduces a CNN-SVM hybrid model for tomato quality grading, achieving 97.50% accuracy in binary and 97.54% in multiclass classifications.	**Image Processing/Artificial Intelligence**
29.	TMMAAI343	**A Novel Framework for Vehicle Detection and Tracking in Night Ware Surveillance Systems** **Objective**: To enhance night-time vehicle detection and tracking, our model employs MIRNet for image enhancement and YOLO with SIFT for accurate tracking.	**Image Processing/Artificial Intelligence**
30.	TMMAAI345	**Classification of Oral Cancer into Pre-Cancerous Stages from White Light Images Using LightGBM Algorithm**	**Image Processing/Artificial Intelligence**

		Objective: The objective of this project is to classify oral cancer into pre-cancerous stages using white light images. Advanced image processing techniques will be applied to extract relevant features, and the LightGBM algorithm will be employed for efficient classification. The model's performance will be evaluated using accuracy metrics to enhance early detection of pre-cancerous conditions.	
31.	**TMMAAN179**	**Design and optimization of a compact microstrip BPF for wireless communication systems based on open-loop rectangular resonators** **Objective**: This project designs a compact microstrip-based Bandpass Filter using open-loop rectangular resonators, achieving low insertion loss and high return loss, simulated in HFSS for efficient 5G and IoT wireless applications.	**Antenna/Reconfigurable Antenna**
32.	**TMMACO178**	**Exploring High-Spin Color Centers in Wide Band Gap Semiconductors SiC: A Comprehensive Magnetic Resonance Investigation (EPR and ENDOR Analysis)** **Objective**: This study characterizes nitrogen–vacancy centers in 4H- and 6H-SiC using high-frequency EPR and ENDOR, revealing spin coherence, optical polarization, and quantum control potential for solid-state qubits and sensors.	**Communications**
33.	**TMMAIP466**	**Enhancing Chronic Disease Prediction in IoMT-Enabled Healthcare 5.0 Using Deep Machine Learning: Alzheimer's Disease as a Case Study** **Objective**: This study proposes an IoMT-enabled deep learning framework using DenseNet-201 for multi-disease classification, achieving high accuracy in pancreatic, brain, and Alzheimer's disease detection, supporting early diagnosis and personalized healthcare.	**Image Processing**
34.	**TMMAIP465**	**Heart Disease Classification from Echocardiogram Images Using Deep Learning** **Objective**: This research develops a modified CNN for automated heart disease classification from echocardiogram images, achieving over 92% accuracy and demonstrating strong potential for clinical decision support in cardiovascular diagnosis.	**Image Processing**

35.	TMMAAI348	**Automated Tool Support for Glaucoma Identification with Explainability Using Fundus Images** **Objective**: The objective of this project is to develop an automated tool for the identification of glaucoma using fundus images, integrating deep learning algorithms to classify the condition. The system will include explainability features to provide clear insights into the decision-making process. This will aid clinicians in understanding and trusting the model's results for better diagnosis.	**Image Processing/Artificial Intelligence**
36.	TMMAIP462	**A Novel Intensity-Corrected Blue Channel Compensation and Edge-Preserving Contrast Enhancement Using Laplace Filter and Sigmoid Function for Sand-Dust Image Enhancement** **Objective**: This study proposes a blue channel compensation and edge-preserving contrast enhancement technique using Laplacian filtering and sigmoid-based saturation adjustment to improve sand-dust image visibility, contrast, and color accuracy.	**Image Processing**
37.	TMMAIP463	**Contrast Limited Adaptive Local Histogram Equalization Method for Poor Contrast Image Enhancement** **Objective:** This study proposes a Contrast Limited Adaptive Local Histogram Equalization (CLALHE) method that adaptively enhances local image contrast, improves visibility, preserves details, and reduces artifacts, validated through qualitative and quantitative metrics.	**Image Processing**
38.	TMMAIP464	**Performance Evaluation of Support Vector Machine and Stacked Autoencoder for Hyperspectral Image Analysis** **Objective:** This study evaluates Support Vector Machine (SVM) and Stacked Autoencoder (SAE) approaches for hyperspectral image classification, highlighting performance differences under varying dataset sizes, noise conditions, and computational constraints.	**Image Processing**
39.	TMMAAN181	**Dynamic Microstrip band pass filter with capacitive coupling for 4G and 5G wireless communication systems** **Objective:** To design and simulate a reconfigurable capacitively coupled microstrip bandpass filter using a PIN diode, enabling dual-frequency operation with low insertion loss and strong impedance matching for 4G LTE and 5G applications.	**Antenna/Reconfigurable Antenna**

40.	TMMACO179	**CONTACTLESS SIMULATION MODEL FOR HUMAN VITAL MONITORING USING UWB RADAR** **Objective:** This project simulates non-contact vital sign monitoring using Ultra-Wideband (UWB) radar in MATLAB, modeling chest motion to detect respiration and heart rate. It enables cost-effective, hardware-free biomedical signal analysis and testing.	**Signal Processing**
41.	TMMAIP460	**Hybrid Image Processing and Deep Learning Framework for Automated Coronary Artery Disease Classification Using Echocardiogram and Angiography** **Objective:** This study presents a hybrid image processing and deep learning framework using enhanced and segmented echocardiogram and angiography images with VGG16 for accurate automated classification of coronary artery disease.	**Image Processing/Artificial Intelligence**
42.	TMMAIP461	**EARLY DETECTION OF FUNGAL DISEASES IN CROPS** **Objective:** This study combines image processing and SVM-based machine learning to accurately detect and classify wheat leaf fungal diseases, enabling early intervention and supporting farmers in effective crop disease management.	**Image Processing/Artificial Intelligence**
43.	TMMAIP459	**DeepSeqCoco: A Robust Mobile Friendly Deep Learning Model for Detection of Diseases in Cocos Nucifera** **Objective**: DeepSeqCoco is a mobile-friendly deep learning framework using EfficientNet-B3 for accurate early detection and classification of five major coconut diseases, enabling automated, reliable, and scalable crop health monitoring.	**Image Processing/Artificial Intelligence**
44.	TMMAIP467	**Recovering the Images Distorted by SurfaceWaves Using an Efficient Multi-Stage Image Reconstruction Strategy** **Objective**: The objective of this study is to develop an efficient multi-stage image reconstruction strategy that accurately restores images distorted by surface waves, enhancing structural clarity, visual quality, and overall image fidelity.	**Image Processing**
45.	TMMAIP468	**Low contrast enhancement algorithm for color image using pythagorean fuzzy sets with a fusion of CLAHE and BPDHE methods** **Objective**: The objective of this study is to enhance low-contrast color images using Pythagorean Fuzzy Sets integrated	**Image Processing**

		with CLAHE and BPDHE, ensuring improved visibility, natural brightness, and color preservation.	
46.	TMMAIP469	**Masked Vascular Structure Segmentation and Completion in Retinal Images** **Objective**: The objective of this study is to develop a U-Net–based deep learning framework for precise retinal blood vessel segmentation, enhancing structural accuracy and connectivity through data augmentation, class weighting, and post-processing techniques.	**Image Processing/Artificial Intelligence**
47.	TMMAIP470	**Comparative Study of Machine Learning and Deep Learning Models for Early Prediction of Ovarian Cancer** **Objective**: The objective of this study is to compare classical machine learning and deep learning models for early ovarian cancer risk prediction using high-dimensional, multi-modal patient data to enhance diagnostic accuracy and personalized care.	**Image Processing/Artificial Intelligence**
48.	TMMAIP471	**Enhancing Hybrid Classification for Plant Diseases with Deep Feature Selection Based on Analytical Entropy and Statistical Method** **Objective**: The objective of this study is to develop an efficient hybrid framework for accurate plant disease classification by integrating deep learning–based feature extraction with entropy-guided feature selection and SVM classification for precision agriculture applications.	**Image Processing/Artificial Intelligence**
49.	TMMAIP472	**Neural-XGBoost: A Hybrid Approach for Disaster Prediction and Management Using Machine Learning** **Objective**: The objective of this study is to develop a hybrid Neural-XGBoost framework that integrates CNN-based deep feature extraction with XGBoost classification for rapid, accurate, and reliable visual disaster type prediction and management.	**Image Processing/Artificial Intelligence**
50.	TMMAIP473	**Classification of Oral Cancer into Pre-Cancerous Stages from White Light Images Using LightGBM Algorithm** **Objective**: The objective of this study is to develop an efficient LightGBM-based framework for classifying oral cancer pre-cancerous stages using multi-color space transformation and feature extraction from white light images to enhance diagnostic accuracy.	**Image Processing/Artificial Intelligence**

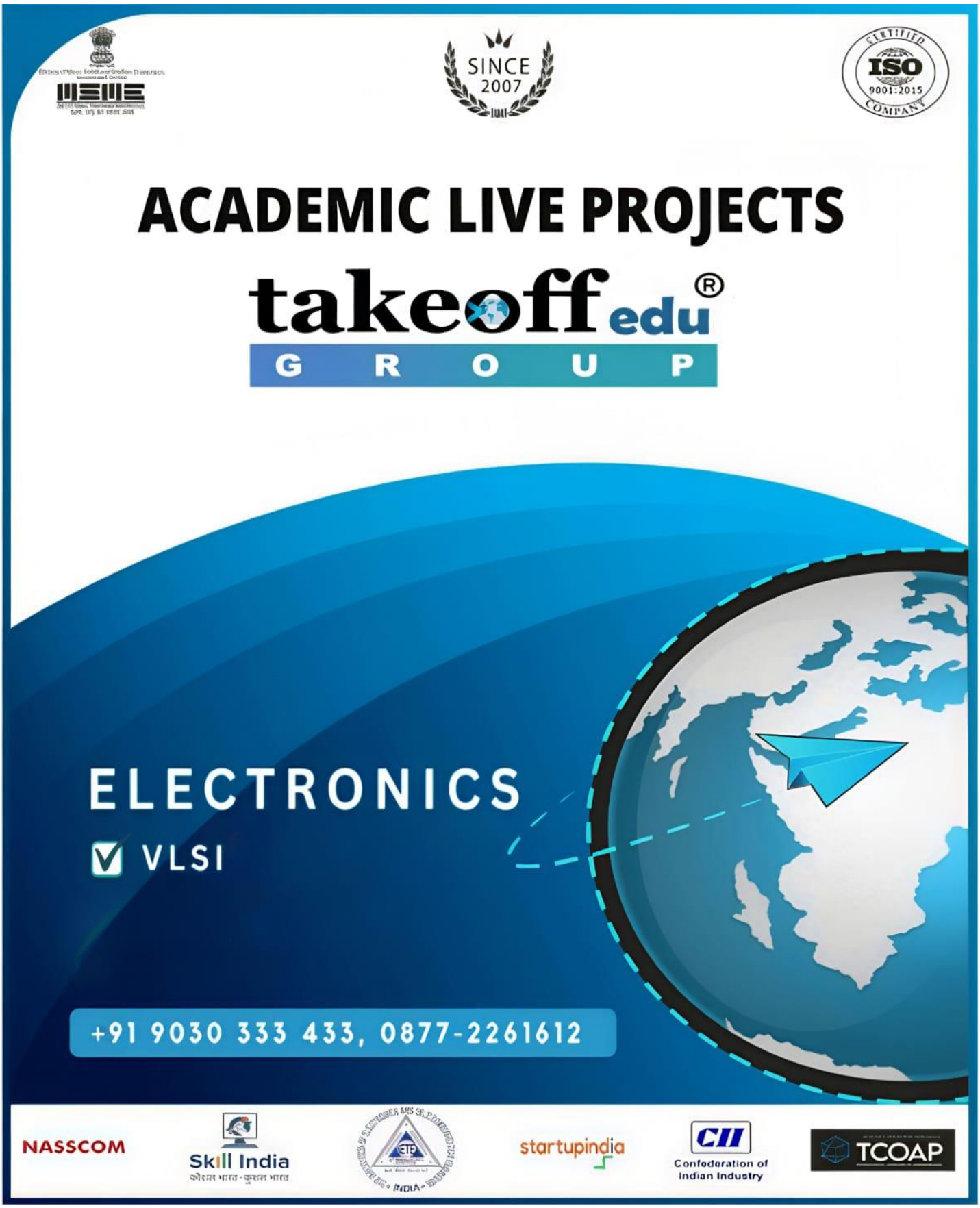
51.	TMMAIP474	**Bone Age Estimation from Hand X-ray Images** **Objective**: The objective of this study is to develop a robust machine learning framework integrating K-Means and KNN classifiers with GLCM feature extraction for accurate identification and multi-stage classification of bone cancer using CT scan images.	**Image Processing/Artificial Intelligence**
52.	TMMAIP475	**Detection of Oral cancer using Image analysis** **Objective**: The objective of this study is to develop a deep learning–based framework integrating ResNet-101 for classification and YOLOv2 for localization to achieve accurate early detection and visualization of oral cancer and potentially malignant disorders.	**Image Processing/Artificial Intelligence**
53.	TMMAIP476	**VGG-16, VGG-16 With Random Forest, Resnet50 With SVM, and EfficientNetB0 with XGBoost-Enhancing Bone Fracture Classification in X-Ray Using Deep Learning Models** **Objective**: The objective of this study is to develop a comparative deep learning framework integrating VGG-16, ResNet-50, and EfficientNetB0 with ensemble classifiers for accurate multi-type bone fracture detection and classification using X-ray images.	**Image Processing/Artificial Intelligence**
54.	TMMACO180	**SVM-Based Enhanced Spectrum Prediction Model for Cognitive Radio Networks** **Objective**: The objective of this study is to develop a CNN-based spectrum prediction model that enhances accuracy, adaptability, and robustness for efficient spectrum utilization in cognitive radio and 5G wireless networks.	**Communications**
55.	TMMACO181	**MACHINE LEARNING-ENHANCED RIS PHASE OPTIMIZATION USING SVD-BASED INITIALIZATION AND MOMENTUM GRADIENT DESCENT IN 6G** **Objective**: The objective of this study is to develop an ML-enhanced RIS phase optimization framework using SVD-based initialization and momentum-based gradient descent to improve convergence speed, spectral efficiency, and energy efficiency in 6G networks.	**Communications**

56.	TMMACO182	**Toward Deployable Multi-Timescale Beamforming for Mobile and Time-Sensitive mm Wave MIMO Networks** **Objective** The objective of this study is to develop a practical multi-timescale cooperative user association and hybrid beamforming protocol with real-time channel estimation and latency-aware scheduling for scalable, low-latency 6G mmWave XL-MIMO networks.	**Communications**
57.	TMMASP223	**Cyber-Resilient Microgrid: Real-time Simulation, Attack Emulation & Secure Monitoring** **Objective:** The objective of this study is to develop a cyber-resilient microgrid framework integrating real-time simulation, cryptographic security, hybrid anomaly detection, and blockchain-based monitoring to enhance reliability and situational awareness against cyber-attacks.	**Communications**
58.	TMMAIP477	**Artificial Intelligence Techniques for Landslides Prediction Using Satellite Imagery** **Objective:** This study aims to develop an accurate landslide prediction system using satellite imagery and a ResNet101 deep learning model to classify regions as landslide-prone or stable for improved environmental risk management.	**Image Processing/Artificial Intelligence**
59.	TMMAIP478	**This study aims to develop an efficient lung disease detection system using a lightweight CNN model that extracts spatial features from chest X-ray images for fast, accurate classification of multiple respiratory conditions.** **Objective:** This study aims to develop an efficient lung disease detection system using a lightweight CNN model that extracts spatial features from chest X-ray images for fast, accurate classification of multiple respiratory conditions.	**Image Processing/Artificial Intelligence**
60.	TMMAIP479	**Deep Learning-Based Multi-Class Model in WSIs: Vision Transformer for Distinguishing Cancer, Tumor, Mitosis, Red Blood Cells, and Karyorrhexis** **Objective:** This study aims to develop a Vision Transformer-based multi-class classification model for accurately identifying diverse cellular structures in whole slide images, enhancing histopathological analysis through robust feature extraction and attention-driven learning.	**Image Processing/Artificial Intelligence**

61.	TMMAIP480	**Breast Cancer Detection Using Mammography:Image Processing to Deep Learning** **Objective:** This study aims to develop an automated breast cancer detection framework using mammography images by integrating deep feature extraction with a meta-learning ensemble classifier to achieve accurate and reliable diagnostic predictions.	**Image Processing/Artificial Intelligence**
62.	TMMAIP481	**3D Reconstruction of X-Ray Skeletal Images** **Objective**: This study aims to develop a three-stage deep learning framework that enhances X-ray images and reconstructs accurate monocular 3D skeletal models for improved clinical interpretation, surgical planning, and diagnostic decision-making.	**Image Processing/Artificial Intelligence**
63.	TMMAIP482	**Adaptive Contrast Enhancement With Lesion Focusing (ACELF)** **Objective**: This study aims to develop an adaptive contrast enhancement algorithm that improves brain MRI visibility and lesion focus, outperforming existing methods in contrast, structural quality, and diagnostic relevance for clinical image pre-processing.	**Image Processing**
64.	TMMAIP483	**Atmospheric Scattering Model Combined With Image Segmentation in Foggy Image Enhancement** **Objective**: This study aims to develop a unified MATLAB framework using the Otsu-ASM algorithm for effective image dehazing, enhancement, and quantitative quality evaluation through automated atmospheric estimation, transmission refinement, and comprehensive metric-based analysis.	**Image Processing**
65.	TMMAIP484	**Brain Tumor Identification and Classification of MRI Images Using Deep Learning Techniques** **Objective**: This study aims to develop a hybrid FAHS–ELM–SVM framework for accurate brain tumor detection and segmentation by enhancing MRI features, optimizing classification, and generating reliable tumor masks with strong diagnostic performance.	**Image Processing/Artificial Intelligence**

66.	TMMACO183	**RFID Secured Intelligent Battery Management System with Predictive Analytics and Cloud Connectivity** **Objective**: This study aims to develop an intelligent MATLAB/Simulink-based battery management system integrating ML-driven SoC/SoH estimation, RFID security, and cloud-enabled diagnostics to enhance accuracy, reliability, and real-time monitoring of EV batteries.	**Communications**
67.	TMMACO184	**A Chaotic Reptile Search Algorithm for Energy Consumption Optimization in Wireless Sensor Networks** **Objective**: This study aims to develop a chaotic Reptile Search Algorithm for energy-efficient WSNs by optimizing cluster head selection, reducing energy consumption, and extending network lifetime compared to existing meta-heuristic approaches.	**Communications**
68.	TMMAIP485	**Classification of Psoriasis Using VisionTransformer: A Deep Learning-Based Approach** **Objective**: This study aims to develop a Vision Transformer–based deep learning model for accurate classification of psoriasis from medical images, improving diagnostic performance over traditional and CNN-based approaches.	**Image Processing/Artificial Intelligence**
69.	TMMAIP488	**Deepfake detection using Convolution Neural Network** **Objective**: This study aims to develop a Convolutional Neural Network–based model for effective detection of deepfake media by learning discriminative visual features that distinguish manipulated content from authentic data.	**Image Processing/Artificial Intelligence**
70.	TMMAIP487	**Pulse Doppler Radar Simulation for Range and Velocity Estimation using MATLAB** **Objective**: This study aims to design and simulate a Pulse Doppler radar system in MATLAB for accurate estimation of target range and velocity through Doppler and time-delay analysis.	**Image Processing/Artificial Intelligence**
71.	TMMAIP486	**Deep UNet Segmentation for High Precision Urban and Environmental Land Cover Classification** **Objective**: This study aims to develop a Deep UNet–based segmentation model for high-precision urban and environmental land cover classification, enabling accurate pixel-level mapping from remote sensing imagery	**Image Processing/Artificial Intelligence**

72.	TMMACO188	**ELECTRONIC COMPONENT FAULT DETETCTION USING MACHINE LEARNING** **Objective**: This study aims to develop a machine learning–based system for accurate detection and classification of electronic component faults, enhancing reliability and reducing diagnostic time compared to conventional methods	**Image Processing/Artificial Intelligence**
73.	TMMACO186	**AI-Driven Predictions for Channel State Information in next generation networks** **Objective**: This study aims to develop AI-driven models for accurate prediction of Channel State Information in next-generation wireless networks, improving communication reliability, spectral efficiency, and network performance.	**Communication**
74.	TMMACO187	**AI-driven intrusion detection system for cloud security** **Objective**: This study aims to develop an AI-driven intrusion detection system for cloud environments that accurately identifies malicious activities and enhances overall cloud security.	**Communication**
75.	TMMAWS142	**Optimizing Routing with ACO and Energy Efficient Localizing with EE LEACH Algorithm** **Objective**: This study aims to optimize network routing using Ant Colony Optimization and enhance energy-efficient localization through the EE-LEACH algorithm, thereby reducing energy consumption and improving network performance.	**Communication**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2025 – 2026 VLSI IEEE TITLES

S.N0	Project I'd	Title	Domain
1.	TVMABE309, TVMABE310	**Analysis of Low area Digital up/down clipping counter for digital In-memory counting** **Objective:** The objective is to design and analyze a low-area digital up/down clipping counter optimized for in-memory computing applications. This involves developing a counter architecture that minimizes silicon area while supporting efficient counting operations with upper and lower bounds (clipping behavior). The focus is on evaluating the counter's performance in terms of area, speed, and power, ensuring its suitability for integration in digital in-memory computing systems where memory and logic are co-located to improve data access efficiency and reduce latency.	BackEnd Domains / Transistor Logic
2.	TVMABE304, TVMABE305	**Design and implementation of 16 Bit SAR ADC for high resolution** **Objective:** Build a high-resolution SAR ADC capable of 16-bit accuracy by leveraging advanced calibration, low-noise comparator and CDAC design, and optimized architecture (segmented CDAC, redundancy, efficient SAR logic), all while maintaining practical speed, low power, and manufacturable silicon performance.	BackEnd Domains / Transistor Logic
3.	TVMABE311	**Experimental Verification and Evaluation of Non-Stateful Logic Gates in Resistive RAM** **Objective:** The objective is to experimentally verify and evaluate the functionality and performance of non-stateful logic gates implemented using Resistive RAM (ReRAM) technology. This includes designing logic gates that operate without storing intermediate logic states, thereby enabling in-memory computing with reduced latency and power consumption. The study aims to assess key metrics such as switching speed, reliability, energy efficiency, and scalability, establishing the potential of non-stateful ReRAM-based logic as a low-power alternative to conventional CMOS logic in emerging computing architectures.	BackEnd Domains / Transistor Logic/ low power

4.	TVMABE318	**Design and Implementation of High-Speed Carry Look-Ahead Decimal Adder (CLDA) Using CMOS Technology** **Objective:** The objective is to design and implement a high-speed Carry Look-Ahead Decimal Adder (CLDA) using CMOS technology for enhanced arithmetic performance in digital systems. The project aims to improve the speed of decimal addition by reducing carry propagation delay through parallel carry generation logic. Using CMOS-based circuit design, the focus is on optimizing parameters such as delay, power consumption, and area, making the adder suitable for high-performance arithmetic units in processors, digital signal processing (DSP), and real-time computing applications.	**BackEnd Domains / Transistor Logic**
5.	TVMABE306, TVMABE307, TVMABE308	**DESIGNING OF ARRAY MULTIPLIER BY USING MEMORY ELEMENT AND MEMRISTOR FOR LOW POWER CONSUMPTION** **Objective:** This project aims to create a low-power, high-density array multiplier by integrating: Memristor crossbar computing for in-memory multiply-accumulate, Hybrid CMOS-memristor cells for logic efficiency.	
6.	TVMAFE653	**Design of Approximate Adder With Reconfigurable Accuracy** **Objective:** To design and implement an approximate adder architecture that allows dynamic or reconfigurable control over its accuracy to achieve an optimal trade-off between power consumption, area, delay, and computational accuracy, especially for error-resilient applications such as image processing, machine learning, and IoT devices.	**Front end Domain / Low power**
7.	TVMAFE655	**Design of Radix-8 Unsigned Bit Pair Recoding Algorithm-Based Floating- Point Multiplier for Neural Network Computations** **Objective:** The primary objective of this project is to design a high-performance floating-point multiplier	**Front end Domain/ Testing**

		based on the Radix-8 Unsigned Bit Pair Recoding algorithm, specifically optimized for neural network computations. Neural networks require a large number of multiply-accumulate operations, making efficient multipliers crucial for accelerating deep learning tasks. The proposed design aims to reduce the number of partial products generated during multiplication by utilizing Radix-8 recoding, thereby minimizing hardware complexity, latency, and power consumption. By maintaining compliance with the IEEE 754 floating-point standard, the design ensures accuracy and compatibility in real-world applications. This multiplier architecture targets hardware platforms such as FPGAs or ASICs, aiming to improve speed, area efficiency, and energy performance in neural network processors. Performance evaluation will include a detailed analysis of delay, power, and resource utilization compared to traditional Radix-2 and Radix-4 designs, demonstrating its suitability for real-time and energy-constrained AI systems.	
8.	**TVMABE319**	**Ternary Toward Binary: Circuit-Level Implementation of Ternary Logic Using Depletion-Mode and Conventional MOSFETs** **Objective:** The objective is to design and implement ternary logic circuits at the transistor level using a combination of depletion-mode and conventional enhancement-mode MOSFETs. This project aims to explore multi-valued logic (MVL) as an alternative to binary logic, focusing on reducing circuit complexity, interconnect overhead, and power consumption. By bridging ternary logic with binary-compatible interfaces, the study evaluates the feasibility, performance, and efficiency of implementing compact, low-power logic circuits suitable for future digital and nanoelectronics systems.	**BackEnd Domains / Transistor Logic/ low power**
9.	**TVMABE320**	**RISC-V CPU Design Using RRAM-CMOS Standard Cells** **Objective:** The objective is to design a RISC-V CPU architecture using hybrid RRAM-CMOS standard cells to	**BackEnd Domains / Transistor Logic/ low power**

		leverage the benefits of non-volatile memory integration in logic design. This project explores the fusion of Resistive RAM (RRAM) with conventional CMOS technology to reduce power consumption, enhance area efficiency, and enable in-memory computing capabilities. The goal is to evaluate the performance, energy efficiency, and scalability of a RISC-V core implemented with RRAM-CMOS logic, aiming to advance energy-efficient processor design for emerging applications such as IoT, edge computing, and neuromorphic systems.	
10.	**TVMABE317**	**Operational Current Amplifier-Based Quadrature Oscillators Family** **Objective:** To develop a systematic family of quadrature oscillator structures by transforming well-known voltage-mode, active-RC oscillator schemes into pure current-mode configurations using OCAs, via the adjoint network theorem.	**Back-end Domain/ Transistor logic**
11.	**TVMABE321**	**Protecting Analog Circuits Using Switch Mode Time Domain Locking** **Objective:** Lock analog circuit behavior by integrating a time-domain switching mechanism controlled by a key. Use random-key–based switching phases instead of conventional fixed-clock signals, ensuring that only with the correct key and correct phase alignment does the analog circuit operate as intended.	**Back-end Domain/ Low power VLSI**
12.	**TVMABE322**	**A High-Speed, Low-Power, High-Reliability and Fully Single Event Double Node Upset Tolerant Design for Magnetic Random Access Memory** **Objective:** High-Speed Operation Enhance read/write access times, making the memory competitive in performance. Low-Power Consumption Minimize the energy required per operation—especially crucial for battery-powered and embedded systems.	**Back-end Domain/ Low power VLSI**

13.	TVMABE323	**A 10-bit 50-MS/s Radiation Tolerant Split Coarse/Fine SAR ADC in 65-nm CMOS** **Objective:** Radiation-Hardened by Design (RHBD): Incorporate robust architecture and circuit-level strategies to mitigate radiation-induced errors (Single Event Effects, Total Ionizing Dose effects, etc.) without resorting to inherently radiation-hardened (and often expensive) fabrication processes.	**Back-end Domain/ Low power VLSI**
14.	TVMAFE664	**Performance Analysis of MAC Unit with Various Parallel Adders** **Objective:** To evaluate the performance of a multiply-accumulate (MAC) unit using different parallel adder architectures to determine trade-offs in speed, area, and power. To identify the best adder choice for MAC-based applications by comparing latency, resource utilization, and energy efficiency across implementations.	**Front end /FPGA**
15.	TVMABE326	**Reliable Multistate RRAM Devices for Reconfigurable CAM and IMC Applications** **Objective:** Integrate these RRAM devices with MOS transistors to build a 4T2R array, enabling reconfigurable analog voltage-based Content-Addressable Memory (CAM) and In-Memory Computing (IMC) accelerators.	**Backend/Nano technology**
16.	TVMABE324 TVMABE325	**A 10bit 50MS per sec Radiation Tolerant Split Coarse or Fine SAR ADC in 65-nm CMOS** **Objective:** Radiation-Hardened by Design (RHBD): Incorporate robust architecture and circuit-level strategies to mitigate radiation-induced errors (Single Event Effects, Total Ionizing Dose effects, etc.) without resorting to inherently radiation-hardened (and often expensive) fabrication processes	**Backend/Nano technology/ Low power**
17.	TVMABE338	**A Low Quiescent Current Fast Transient LDO Regulator With Segmented Pass Transistors**	**Backend/Nano technology/ Low power**

		Objective: The main objective of this work is to design and implement a low dropout (LDO) voltage regulator that achieves low quiescent current while providing fast transient response during rapid load variations. The regulator aims to balance power efficiency and stability by using segmented pass transistors to dynamically adjust the drive strength according to the load current demand. This approach minimizes power loss under light loads while maintaining high performance and quick settling under heavy load conditions.	
18.	**TVMABE341**	**Robust and Reliable Energy-Efficient Level Shifter** **Objective:** The objective of this work is to design a robust and energy-efficient level shifter that reliably converts low-voltage logic signals to higher voltage levels with minimal power consumption and reduced delay. The design aims to achieve high performance, noise immunity, and process variation tolerance while maintaining stable operation across wide voltage ranges, making it suitable for low-power and multi-voltage VLSI systems.	**Backend/ Low power**
19.	**TVMAFE668**	**Design of generic vedic ALU using reversible logic** **Objective:** The objective of this work is to design a generic Arithmetic Logic Unit (ALU) based on Vedic mathematics and implemented using reversible logic to achieve low power consumption, reduced circuit complexity, and high computational efficiency. The design focuses on combining Vedic arithmetic techniques with reversible logic gates to minimize energy dissipation and improve the speed and scalability of arithmetic operations in future low-power and quantum computing systems.	**Front end/ Arthematic**
20.	**TVMAFE666**	**High-Speed CMOS Synchronous Binary Counter With Constant Counting Rate** **Objective:** The objective of this work is to design and implement a CMOS-based synchronous binary counter capable of operating at high speed while maintaining a	**Front end/ Communication**

		constant counting rate across all bit stages. The design focuses on reducing propagation delay, enhancing switching performance, and ensuring uniform timing by optimizing the counter's logic structure. This approach enables efficient and reliable operation in high-frequency and low-power digital systems.	
21.	**TVMAFE669**	**Design and Implementation of Single Master Single Slave Serial Peripheral Interface (SPI) on FPGA** **Objective:** The main objective of this project is to design, implement, and verify a Single Master–Single Slave Serial Peripheral Interface (SPI) communication protocol using FPGA to achieve high-speed, reliable, and synchronous serial data transfer between digital devices. The project aims to model the SPI architecture in hardware description language (HDL), simulate its functional behavior, and implement it on an FPGA board to validate real-time performance and communication accuracy.	**Front end/ Communication**
22.	**TVMAFE671** **TVMAFE670**	**Design and Implementation of Modified Carry Select Adder** **Objective:** The main objective of this project is to design, implement, and analyze a Modified Carry Select Adder (MCSA) architecture to achieve high-speed and low-power arithmetic operation compared to the conventional Carry Select Adder. The project focuses on optimizing delay, area, and power by reducing redundant computations and improving carry propagation efficiency. The design will be modeled using HDL, simulated for functional correctness, and implemented on FPGA to validate performance improvements.	**Front end/ Communication, Arthematic**
23.	**TVMAFE672**	**Verification of AMBA APB Bus Protocol Using UVM** **Objective:** The main objective of this project is to verify the functionality of the AMBA Advanced Peripheral Bus (APB) protocol using the Universal Verification Methodology (UVM) to ensure reliable and efficient	**Front end/ Communication**

		data communication between peripherals in a System-on-Chip (SoC) design. The project aims to develop a reusable, modular, and coverage-driven UVM-based verification environment to validate protocol compliance, functionality, and performance of the APB interface.	
24.	TVMAFE673	**Synthesis of AMBA APB BUS Protocol** **Objective:** The objective of the project "Synthesis of AMBA APB Bus Protocol" is to design, implement, and synthesize an efficient communication interface based on the Advanced Microcontroller Bus Architecture (AMBA) Advanced Peripheral Bus (APB) standard. The main goal is to enable reliable and low-power data transfer between the processor and various peripheral devices in a System-on-Chip (SoC) design. This involves developing the APB master and slave modules, verifying their functionality through simulation, and synthesizing the design to evaluate performance parameters such as area, timing, and power. The project aims to achieve a simple, cost-effective, and high-performance bus interface suitable for low-bandwidth peripheral communication in embedded systems.	**Front end/ Communication**
25.	TVMAFE674	**Design and Implementation of SRAM on FPGA and Verification Using UVM** **Objective:** The objective of this project is to design and implement a Static Random Access Memory (SRAM) on an FPGA platform to achieve high-speed and efficient data storage. It focuses on developing a memory architecture with optimized area and power utilization. The design will be synthesized, implemented, and tested on FPGA hardware to verify its functionality and performance. Universal Verification Methodology (UVM) is used to create a reusable and robust verification environment. The goal is to ensure the correctness, reliability, and efficiency of the SRAM design through functional and timing verification.	**Front end/FPGA**

26.	TVMAFE675	**Design and implementation of MOD60 counter based on Multisim** **Objective:** The objective of this project is to design and implement a MOD60 counter using Multisim for accurate counting and timing applications. It focuses on developing a digital counter capable of counting from 0 to 59 and resetting automatically after reaching the maximum count. The design will be created and simulated in Multisim to verify its functional correctness and timing behavior. The project aims to optimize the circuit for simplicity, reliability, and low power consumption. The overall goal is to demonstrate the practical realization of sequential digital logic design using simulation tools.	**Front end/FPGA**
27.	TVMAFE676	**Arithmetic Logic Unit using 4-bit Vedic Multipliers with Multiplexers** **Objective:** The objective of this project is to design and implement an Arithmetic Logic Unit (ALU) using 4-bit Vedic multipliers integrated with multiplexers for efficient arithmetic and logical operations. It focuses on enhancing the speed and performance of the ALU by utilizing the Urdhva Tiryakbhayam sutra from Vedic mathematics. The design will be simulated and verified to ensure accurate functionality and reduced computational delay. Multiplexers are used to select between different operations, improving flexibility and control. The overall goal is to develop a high-performance, low-latency ALU suitable for modern digital processing applications.	**Front end/FPGA**
28.	TVMABE342, TVMABE343, TVMABE344, TVMABE345	**Design and Simulation of a Carry Save Adder (CSA) using NAND Gate in CMOS 180nm Technology** **Objective:** The objective of this project is to design and simulate a Carry Save Adder (CSA) using NAND gates in CMOS 180nm technology for high-speed arithmetic computation. It focuses on optimizing the adder design to achieve reduced propagation delay and efficient power utilization. The CSA will be implemented using only NAND gates to demonstrate the universality and	**Backend/low power/ nano technology/ cadence**

		compactness of logic design. Simulation will be performed to verify functionality, timing, and power performance at the transistor level. The overall goal is to develop a fast and area-efficient adder architecture suitable for VLSI and digital signal processing applications.	
29.	TVMAFE677	**Design of 8 bit Arithmetic Logic Unit for Signal Processing Applications using Verilog** **Objective:** The objective of this project is to design and implement an 8-bit Arithmetic Logic Unit (ALU) using Verilog for efficient signal processing applications. It focuses on performing various arithmetic and logical operations with high speed and accuracy. The design will be simulated and verified to ensure correct functionality and optimized performance in digital computation. Special attention is given to minimizing delay and power consumption while maintaining design flexibility. The overall goal is to develop a reliable and high-performance ALU suitable for integration into signal processing and embedded system architectures.	**Front end/FPGA**
30.	TVMAFE678	**Design and Analysis of Different Adders Using Reversible Logic Gates** **Objective:** The objective of this project is to design and analyze different adder circuits using reversible logic gates for low-power and energy-efficient computation. It focuses on implementing adders such as ripple carry, carry look-ahead, and carry save using reversible gates to minimize information loss. The design will be simulated to evaluate parameters like delay, power consumption, and gate count. Reversible logic is applied to achieve reduced heat dissipation and improved performance in digital circuits. The overall goal is to develop optimized adder architectures suitable for future low-power and quantum computing applications.	**Front end/FPGA**
31.	TVMAFE679	**Approximate Parallel Prefix Adders for Image Processing Applications**	**Front end/Arithmetic**

		Objective: The objective of this project is to design and develop approximate parallel prefix adders aimed at achieving efficient and high-speed performance for image processing applications. The focus is on optimizing the trade-off between computational accuracy, power consumption, and delay through controlled approximation techniques. Various parallel prefix adder architectures will be designed, analyzed, and compared based on key performance parameters such as area, delay, and power. Simulation and verification will be performed to ensure the functional correctness and efficiency of the proposed designs. The ultimate goal is to realize low-power, high-performance adders suitable for real-time image and multimedia processing systems.	**core**
32.	**TVMAFE680**	**Wallace Tree Multiplier Using Reversible Logic With Brent-Kung Adder** **Objective:** The objective of this project is to design and implement a Wallace Tree Multiplier using reversible logic integrated with a Brent-Kung adder for high-speed and low-power arithmetic operations. It focuses on optimizing multiplication performance by reducing delay and power dissipation through reversible logic design. The Brent-Kung adder is employed to enhance addition efficiency and minimize circuit complexity. Simulation and analysis will be carried out to evaluate parameters such as area, delay, and power consumption. The overall goal is to develop an energy-efficient and high-performance multiplier architecture suitable for advanced digital and VLSI applications.	**Front end/Arithmetic core**
33.	**TVMAFE681**	**Design and Analysis of 4-bit and 8-bit Vedic Multipliers Using Variable Bit CSLA** **Objective:** The objective of this project is to design and analyze 4-bit and 8-bit Vedic multipliers using a variable bit Carry Select Adder (CSLA) for high-speed arithmetic operations. It focuses on improving computational efficiency by combining the advantages of Vedic	**Front end/Arithmetic core**

		mathematics and optimized adder architecture. The design will be implemented and simulated to evaluate key performance parameters such as delay, power, and area. Comparative analysis will be conducted between 4-bit and 8-bit implementations to study scalability and performance improvement. The overall goal is to develop a fast, low-power, and area-efficient multiplier suitable for modern digital and signal processing applications.	
34.	**TVMAFE682**	**8-Bit Approximate Multiplier using Approximate Full Adder** **Objective:** The objective of this project is to design and implement an 8-bit approximate multiplier using approximate full adders for high-speed and power-efficient arithmetic operations. It focuses on reducing computational complexity and power consumption by introducing controlled approximation in the multiplier design. The circuit will be modeled and simulated to evaluate key performance parameters such as delay, area, and power. Functional verification will be performed to ensure acceptable accuracy levels for practical applications. The overall goal is to develop a low-power, high-performance approximate multiplier suitable for image processing and error-tolerant computing systems.	**Front end/Arithmetic core**
35.	**TVMAFE683**	**Implementation of FIR Filter Using Different Adder Architectures** **Objective:** The objective of this project is to design and implement a Finite Impulse Response (FIR) filter using different adder architectures for efficient digital signal processing. It focuses on analyzing the impact of various adders on the filter's speed, power consumption, and hardware complexity. Different adder structures such as Ripple Carry, Carry Look-Ahead, and Carry Save Adders will be implemented and compared. Simulation and verification will be carried out to evaluate the filter's performance in terms of delay, area, and power. The overall goal is to develop	**Front end/Arithmetic core**

		an optimized FIR filter design suitable for high-speed and low-power signal processing applications.	
36.	TVMAFE684	**Enhancing Performance of Floating-Point Units Using Parallel Prefix Adders** **Objective:** The objective of this project is to design and implement an optimized Floating-Point Unit (FPU) using parallel prefix adders to enhance computational speed and efficiency. It focuses on improving arithmetic operation performance by integrating high-speed adder architectures into the FPU design. Different parallel prefix structures such as Kogge-Stone and Brent-Kung adders will be analyzed and compared based on delay, area, and power consumption. Simulation and verification will be performed to validate the functional accuracy and performance improvements. The overall goal is to develop a high-performance, low-latency FPU suitable for advanced digital and signal processing applications.	**Front end/Arithmetic core**
37.	TVMAFE685	**Design and Implementation of a Secure and Accurate Electronic Voting Machine using Verilog on Zynq FPGA** **Objective:** The objective of this project is to design and implement a secure and accurate electronic voting machine using Verilog on a Zynq FPGA platform. It focuses on developing a reliable digital system that ensures voter privacy, data integrity, and accurate vote counting. The design will incorporate security features such as authentication and error detection to prevent tampering and unauthorized access. Simulation and hardware implementation on FPGA will be carried out to verify functionality and performance. The overall goal is to create a robust, efficient, and tamper-resistant voting system suitable for real-time election applications.	**Front end/FPGA**
38.	TVMAFE686	**A Novel BIST Method for Multi-Port Register Files** **Objective:** The objective of this project is to design and implement a novel Built-In Self-Test (BIST) method for	**Front end/FPGA**

		multi-port register files to enhance testing efficiency and fault detection capability. It focuses on developing a self-testing architecture that reduces external testing complexity and improves reliability. The proposed BIST scheme will be analyzed for parameters such as fault coverage, area overhead, and testing time. Simulation and verification will be performed to validate the functionality and effectiveness of the design. The overall goal is to achieve a high-performance, low-cost, and reliable testing solution for modern VLSI register file architectures.	
39.	TVMAFE687	**Design of a Power-Aware Reconfigurable and Parameterizable Pseudorandom Pattern Generator for BIST-Based Applications** **Objective:** The objective of this project is to design and implement a power-aware, reconfigurable, and parameterizable pseudorandom pattern generator (PRPG) for BIST-based applications. It focuses on reducing power consumption while maintaining high fault coverage and flexibility in test pattern generation. The design will allow reconfiguration of parameters such as seed values and sequence length to support diverse testing requirements. Simulation and analysis will be carried out to evaluate performance metrics like power, area, and test efficiency. The overall goal is to develop an energy-efficient and adaptable PRPG architecture suitable for modern low-power VLSI testing environments.	**Front end/FPGA**
40.	TVMAFE688	**Implementation of Memory Built-In Self-Test** **Objective:** The objective of this project is to design and implement a Memory Built-In Self-Test (MBIST) architecture for efficient testing and fault detection in embedded memory systems. It focuses on developing a self-test mechanism that can identify common memory faults such as stuck-at, transition, and coupling faults without external testing equipment. The design will be simulated and verified to ensure high fault coverage, low area overhead, and reliable performance. Different	**Front end/FPGA**

		test algorithms will be analyzed to optimize testing time and accuracy. The overall goal is to create a cost-effective and efficient MBIST solution suitable for modern VLSI and SoC applications.	
41.	**TVMAFE689**	**Efficient Architectures of FIR Filters using Distributed Arithmetic** **Objective:** The objective of this project is to design and implement efficient architectures of FIR filters using distributed arithmetic for high-speed and low-power digital signal processing applications. It focuses on optimizing computation by replacing multipliers with look-up tables and adders to reduce hardware complexity. Different FIR filter architectures will be analyzed and compared based on performance metrics such as area, delay, and power consumption. Simulation and verification will be carried out to ensure functional accuracy and efficiency. The overall goal is to develop compact, high-performance FIR filter designs suitable for real-time signal processing systems.	**Front end/Arithmetic core**
42.	**TVMAFE691**	**Implementation of Digital FIR Filter Using Optimized Hybrid Arithmetic Unit** **Objective:** The objective of this project is to design and implement a digital FIR filter using an optimized hybrid arithmetic unit for high-speed and low-power signal processing applications. It focuses on enhancing filter performance by combining different arithmetic techniques to reduce computational delay and hardware complexity. The design will be simulated and verified to evaluate key parameters such as area, power consumption, and processing speed. Comparative analysis will be performed to demonstrate improvements over conventional FIR filter implementations. The overall goal is to develop an efficient, reliable, and high-performance FIR filter suitable for real-time digital signal processing systems.	**Front end/Arithmetic core**
43.	**TVMAFE692**	**A Comparative Study between FPGA and DSP for the Efficient Implementation of FIR Filters**	**Front end/FPGA & DSP Core**

		Objective: The objective of this project is to perform a comparative study between FPGA and DSP platforms for the efficient implementation of FIR filters. It focuses on analyzing performance metrics such as speed, power consumption, area utilization, and computational efficiency on both platforms. FIR filters will be designed, implemented, and simulated on FPGA and DSP to evaluate their respective advantages and limitations. The study aims to identify the most suitable platform for different signal processing applications based on design requirements. The overall goal is to provide insights into optimizing FIR filter implementation for high-performance and low-power digital systems.	
44.	**TVMAFE694**	**Analysis of 8x8 Bit Various Multiplier Using Look-Up Table and Implementation in Fir Filter** **Objective:** The objective of this project is to design and analyze 8×8-bit multipliers using look-up table (LUT) techniques and implement them in FIR filters for efficient digital signal processing. It focuses on optimizing multiplication operations to reduce hardware complexity, delay, and power consumption. Different multiplier architectures will be compared and evaluated based on performance metrics such as speed, area, and power efficiency. The design will be integrated into FIR filter implementation and simulated to verify functional accuracy and performance improvement. The overall goal is to develop a high-speed, low-power multiplier-based FIR filter suitable for real-time signal processing applications.	**Front end/Arithmetic core**
45.	**TVMAFE695**	**FPGA Implementation of an Efficient FIR Filter Using Double MAC Unit** **Objective:** The objective of this project is to design and implement an efficient FIR filter on FPGA using a double MAC (Multiply-Accumulate) unit to enhance computational speed and throughput. It focuses on optimizing filter performance by performing parallel multiply-accumulate operations, reducing processing	**Front end/Arithmetic core**

		time and hardware utilization. The design will be simulated and verified to evaluate key parameters such as area, power consumption, and processing efficiency. Comparative analysis will be conducted to demonstrate improvements over conventional single-MAC FIR filter implementations. The overall goal is to develop a high-performance, low-latency FIR filter suitable for real-time digital signal processing applications.	
46.	**TVMAFE696**	**Modified FIR Filter and High Speed Adder for Signal Processing Applications** **Objective:** The objective of this project is to design and implement a modified FIR filter integrated with a high-speed adder for efficient signal processing applications. It focuses on enhancing the filter's performance by reducing computational delay and improving processing speed through optimized adder architecture. The design will be simulated and verified to evaluate key parameters such as area, power consumption, and accuracy. Comparative analysis will be carried out to demonstrate improvements over conventional FIR filter and adder implementations. The overall goal is to develop a high-performance, low-latency, and energy-efficient FIR filter suitable for real-time digital signal processing systems.	**Front end/Arithmetic core**
47.	**TVMAFE697**	**Design and Analysis of 4x4 bit various Multiplier Using Look-up table and implementation in FIR Filter** **Objective:** The objective of this project is to design and analyze 4×4-bit multipliers using look-up table (LUT) techniques and implement them in FIR filters for efficient digital signal processing. It focuses on optimizing multiplication operations to reduce hardware complexity, delay, and power consumption. Different 4×4-bit multiplier architectures will be compared based on performance metrics such as speed, area, and power efficiency. The design will be integrated into FIR filter implementation and simulated to verify functional correctness and performance improvement. The overall goal is to develop a compact,	**Front end/Arithmetic core**

		high-speed, and low-power multiplier-based FIR filter suitable for real-time signal processing applications.	
48.	TVMAFE698	**Implementation of FIR Filter Using Wallace Reduction Tree For High Speed Application** **Objective:** The objective of this project is to design and implement a FIR filter using a Wallace Reduction Tree to achieve high-speed performance in digital signal processing applications. It aims to speed up multiplication operations by efficiently reducing partial products through the Wallace tree structure, thereby minimizing processing delay. The design will be simulated and analyzed to assess key performance metrics such as speed, area, and power consumption. A comparative study will be conducted to highlight the improvements over traditional FIR filter implementations. The overall goal is to develop a fast, low-latency, and efficient FIR filter suitable for real-time high-speed signal processing systems.	**Front end/Arithmetic core**
49.	TVMABE346	**Stacked Ring Oscillators with Fractional Injection Lock** **Objective:** The objective of this project is to design and implement stacked ring oscillators with fractional injection lock to achieve precise frequency control and improved performance in high-speed electronic circuits. It focuses on enhancing oscillator stability and tuning range by leveraging fractional injection locking techniques. The design will be simulated and analyzed to evaluate key parameters such as frequency accuracy, phase noise, and power consumption. Comparative analysis will be carried out to demonstrate improvements over conventional ring oscillator designs. The overall goal is to develop a high-performance, low-power oscillator suitable for advanced communication and signal processing applications.	**Backend/ Low power VLSI**
50.	TVMABE347	**A Transformer Feedback Oscillator** **Objective:** The objective of this project is to design and	**Backend/ Transistor logic**

		implement a transformer feedback oscillator to achieve stable and efficient sinusoidal signal generation. It focuses on utilizing transformer feedback to maintain oscillations with low distortion and consistent amplitude. The design will be simulated and analyzed to evaluate key parameters such as frequency stability, output amplitude, and power consumption. Comparative analysis may be performed to highlight advantages over conventional oscillator circuits. The overall goal is to develop a reliable, high-performance oscillator suitable for communication and signal processing applications.	
51.	TVMABE348	**A dB-Linear Programmable Gain Amplifier With Mixed-Signal Control for Wide-Gain Range and Low-Power Applications** **Objective:** The objective of this project is to design and implement a dB-linear programmable gain amplifier (PGA) with mixed-signal control to achieve a wide gain range while maintaining low power consumption. It focuses on providing precise and linear gain adjustment through a combination of analog and digital control techniques. The design will be simulated and analyzed to evaluate performance metrics such as gain accuracy, linearity, bandwidth, and power efficiency. Comparative analysis will be carried out to demonstrate improvements over conventional PGA designs. The overall goal is to develop a high-performance, low-power, and versatile amplifier suitable for modern mixed-signal and communication applications.	**Backend/ Cadence**
52.	TVMABE349, TVMABE350, TVMABE351, TVMABE352	**Design Considerations of High- Frequency-Reference Fractional- N PLL: Architecture and Nonidealities** **Objective:** The objective of this project is to study and design a high-frequency-reference fractional-N Phase-Locked Loop (PLL), focusing on its architecture and the impact of nonidealities on performance. It aims to optimize the PLL for stable frequency synthesis, low phase noise, and fast lock time in high-frequency applications. The design and analysis will consider nonideal effects such as jitter, reference spurs, and component mismatches to	**Backend/ Cadence/ Low power VLSI/ Transistor logic/ Nano technology**

		improve overall reliability. Simulation and evaluation will be carried out to assess key parameters including frequency accuracy, stability, and power consumption. The overall goal is to develop a robust and high-performance fractional-N PLL suitable for modern communication and signal processing systems.	
53.	**TVMABE353, TVMABE354**	**Comparative Analysis of XOR Implementation using CMOS Logic, Domino Logic - Keeper Technique** **Objective:** The objective of this project is to design and perform a comparative analysis of XOR gate implementations using CMOS logic and Domino Logic with the keeper technique. It focuses on evaluating the performance differences in terms of speed, power consumption, and area between conventional CMOS and Domino Logic designs. The designs will be simulated to verify functionality and measure key parameters such as propagation delay, dynamic power, and robustness. Comparative study will highlight the advantages and trade-offs of each approach for high-speed digital circuits. The overall goal is to identify the most efficient XOR gate implementation suitable for modern VLSI and high-performance digital applications.	**Backend/ Cadence/ Low power VLSI**
54.	**TVMABE355, TVMABE356, TVMABE357**	**Comparative Study of Transistor Logic Families in Half Adder Circuit Design** **Objective:** The objective of this project is to design a half adder circuit using various transistor logic families and conduct a comparative study of their performance. It focuses on evaluating parameters such as speed, power consumption, propagation delay, and circuit area for different logic families including CMOS, PTL, and Domino logic. The designs will be simulated and verified to ensure correct functionality and to measure performance accurately. Comparative analysis will highlight the strengths and limitations of each logic family in arithmetic circuit design. The overall goal is to determine the most efficient and reliable logic family for high-performance digital circuits.	**Backend/ Low power VLSI/ Transistor logic**

55.	TVMABE361	**Cascode voltage switch logic: A differential CMOS logic family** **Objective:** The objective of this project is to design and analyze a Cascode Voltage Switch Logic (CVSL) differential CMOS logic family for high-speed and low-power digital circuit applications. It focuses on leveraging differential operation to achieve faster switching, reduced noise, and improved signal integrity compared to conventional CMOS logic. The design will be simulated and evaluated for key parameters such as propagation delay, power consumption, and noise margin. Comparative analysis will be carried out to demonstrate the advantages of CVSL over traditional single-ended logic families. The overall goal is to develop a high-performance, energy-efficient logic design suitable for advanced VLSI and high-speed digital systems.	**Backend/ Nano technology**
56.	TVMABE358, TVMABE359, TVMABE360	**Design and Comparative Analysis of Half and Full Adders Using CMOS and Pass Transistor Logic Styles** **Objective:** The objective of this project is to design half and full adder circuits using CMOS and Pass Transistor Logic (PTL) styles and perform a comparative analysis of their performance. It focuses on evaluating key parameters such as propagation delay, power consumption, transistor count, and circuit area for both logic styles. The designs will be simulated and verified to ensure functional correctness and to accurately measure performance metrics. Comparative analysis will highlight the advantages and trade-offs of CMOS and PTL implementations in arithmetic circuit design. The overall goal is to identify the most efficient and reliable adder design suitable for high-performance digital applications.	**Backend/ Low power VLSI/ Transistor logic**
57.	TVMABE362, TVMABE363	**Design and Performance Analysis of CMOS, GDI, and PTL Logic Gates at 90nm Technology** **Objective:** The objective of this project is to design and analyze logic gates using CMOS, Gate Diffusion Input (GDI), and Pass Transistor Logic (PTL) styles at 90nm technology. It focuses on evaluating key performance parameters such as propagation delay, power consumption, area, and noise margin for each logic style. The designs will be simulated	**Backend/ Low power VLSI/ Transistor logic**

		and verified to ensure correct functionality and to measure efficiency accurately. Comparative analysis will highlight the strengths, weaknesses, and trade-offs of CMOS, GDI, and PTL implementations. The overall goal is to identify the most efficient and high-performance logic gate design suitable for advanced VLSI circuits.	
58.	**TVMABE364, TVMABE365**	**Combinational and Sequential Design Logic for Ternary System** **Objective:** The objective of this project is to design and implement combinational and sequential logic circuits for a ternary (three-valued) system to explore alternatives to conventional binary logic. It focuses on developing ternary logic circuits that can perform arithmetic and control operations with reduced hardware complexity and improved data density. The designs will be simulated and verified to evaluate key performance parameters such as speed, power consumption, and circuit area. Comparative analysis may be conducted to assess the efficiency and advantages of ternary logic over binary systems. The overall goal is to develop high-performance, compact, and efficient ternary logic circuits suitable for advanced digital and VLSI applications.	**Backend/ Low power VLSI/ Transistor logic**
59.	**TVMABE366, TVMABE367**	**A Low-Power Low-Voltage Binary Search Analog-to-Digital Converter** **Objective:** The objective of this project is to design and implement a low-power, low-voltage binary search analog-to-digital converter (ADC) for energy-efficient signal conversion applications. It focuses on achieving high-speed and accurate digital output while minimizing power consumption and operating voltage. The design will be simulated and analyzed to evaluate key performance metrics such as resolution, conversion time, linearity, and power efficiency. Comparative analysis may be conducted to highlight improvements over conventional ADC designs. The overall goal is to develop a compact, high-performance, and low-power ADC suitable for modern portable and low-energy electronic systems.	**Backend/ Low power VLSI/ Cadence**

60.	TVMABE368, TVMABE369	**Adept Domino Logic for Modified Schmitt Trigger Circuits** **Objective:** The objective of this project is to design and implement Adept Domino Logic for modified Schmitt Trigger circuits to achieve high-speed and noise-immune digital performance. It focuses on enhancing signal integrity and reducing propagation delay by combining the advantages of domino logic with Schmitt Trigger characteristics. The design will be simulated and analyzed to evaluate key parameters such as speed, power consumption, noise margin, and robustness. Comparative analysis will be performed to demonstrate improvements over conventional Schmitt Trigger and standard domino logic implementations. The overall goal is to develop a fast, reliable, and low-power circuit suitable for high-performance VLSI applications.	**Backend/ Low power VLSI/ Cadence**
61.	TVMABE370, TVMABE371	**A Low-Dropout, High-Current LDO Design** **Objective:** The objective of this project is to design and implement a low-dropout (LDO) regulator that can provide high current with minimal voltage drop and high efficiency. It aims to achieve stable voltage regulation, quick transient response, and low power dissipation for modern electronic applications. The design will be simulated and analyzed to assess key performance parameters such as output voltage accuracy, dropout voltage, load regulation, and overall power efficiency. Comparative evaluation may be performed to demonstrate improvements over conventional LDO designs. The overall goal is to develop a high-performance, reliable, and energy-efficient LDO suitable for powering high-current integrated circuits and electronic systems.	**Backend/ Low power VLSI/ Cadence**
62.	TVMAFE702	**Design and Implementation of an Adaptive FPGA-Based Traffic Light Control System Using Verilog** **Objective:** Adaptive Signal Timing Based on Traffic Conditions • Dynamically adjust traffic light durations (green, yellow, red) according to real-time traffic density rather than using a fixed timer.	**Front End Domains FPGA**

		• Use sensors (vehicle detectors) to estimate traffic flow and modify signal phases to reduce congestion.	
63.	TVMAFE703	**Implementation of an Enhanced RC6 Algorithm for Securing Data Using Verilog** **Objective:** Enhance Security over Standard RC6 • Implement a modified (or "enhanced") version of RC6 such that its resistance to cryptanalysis (like differential or linear cryptanalysis) is improved. For example, some "enhanced RC6" variants use more complex diffusion or "box"-type operations to increase security. • Possibly introduce symmetric layers or additional algebraic transformations to break simple relationships, which strengthens the cipher.	**Front End Domains DSP Core**
64.	TVMAFE700	**Design of Asynchronous FIFO with Adjustable Input-Output Bit Width Based on Verilog** **Objective:** Optimized for High-Speed Data Transfer • The design aims to maintain high-speed performance even when performing bit-width conversion. • Ensuring that the FIFO's control logic and memory structure do not become a bottleneck in high-throughput scenarios.	**Front End Domains/ Arithmetic Core**
65.	TVMABE372, TVMABE373	**Reversible logic circuit design using QCA based modified Fredkin gate.** **Objective:** Design a Modified Fredkin Gate in QCA • Propose a new layout / architecture of the Fredkin gate using Quantum-Dot Cellular Automata (QCA), improving on prior designs. • Ensure that the modified Fredkin gate is *reversible* (i.e., bijective mapping of inputs to outputs) to minimize information loss.	**Back End Domains Core Memories / Low Power VLSI**
66.	TVMAFE704	**Design and Implementation of Asynchronous Counter Using Reversible Logic Gates**	**Front End Domains Arithmetic Core**

		Objective: Reduce Power Dissipation • Use reversible logic because it ideally conserves information, leading to lower energy loss (heat) compared to irreversible circuits. • Specifically, target lower power consumption in the asynchronous counter by using reversible flip-flops.	
67.	**TVMAFE701**	**REALIZATION OF LOW POWER AND EFFICIENT SEQUENTIAL CIRCUITS USING REVERSIBLE LOGIC GATES** **Objective:** Reduce Power Dissipation • Since reversible logic ideally conserves information, it can significantly lower energy loss in sequential circuits. • Applying reversible gates (like Toffoli, Fredkin, Peres, etc.) in flip-flops or counters aims to minimize the usual power consumption associated with conventional (irreversible) logic.	**Front End Domains/ Arithmetic Core**
68.	**TVMAFE705**	**Design And Implementation Of Power Efficient Multiplier Using Reversible Logic** **Objective:** Reduce Power Dissipation • Use reversible logic to lower energy loss, since reversible gates ideally avoid bit erasure and thus reduce heat / power dissipation. • Target ultra-low power, which is especially relevant in future VLSI, quantum, or nanocomputing contexts.	**Front End Domains Arithmetic Core**
69.	**TVMAFE699**	**Design for Testability in VlSI** **Objective:** 1. By adding testability features (e.g., scan, BIST), you can reduce dependence on expensive external testers, reduce the number of test patterns, and speed up testing. 2. Use ATPG (Automated Test Pattern Generation) to optimize and minimize the required test vectors.	**Major Projects / Front End Domains/ DSP Core**
70.	**TVMAFE706**	**Design & Verification of Reconfigurable SRAM Controller with AMBA AXI Protocol Interface for Automobile Application**	**Front End Domains Communications**

		Objective: Develop a Reconfigurable SRAM Controller • To design an SRAM controller whose behavior/configuration can adapt to different requirements (e.g., memory size, access patterns) — "reconfigurable" means it's not a fixed, one-size-fits-all controller. • Make this controller suitable for automotive systems, which often have varying memory demands depending on the subsystem (infotainment, ADAS, etc.).	
71.	**TVMAFE707**	**FPGA based UART Design: Simulation, Synthesis & System Verilog functional verification** **Objective:** Implement a UART (Universal Asynchronous Receiver/Transmitter) on FPGA • Design a UART transmitter (TX) and receiver (RX) module in HDL (SystemVerilog or Verilog), so that serial communication (asynchronous) can be achieved. • Provide configurable parameters for UART, like baud rate, data bits, parity, and stop bits. (Many designs include a baud-rate generator.) • Use FPGA hardware (e.g., a Xilinx or Intel/Altera board) to demonstrate real, physical serial communication	**Front End Domains Communications**
72.	**TVMAFE708**	**Designing of AES-128 Encryption Algorithm Using System Verilog VLSI** **Objective:** Hardware Realization of AES-128 • Implement the full AES-128 algorithm (10 rounds of SubBytes, ShiftRows, MixColumns, AddRoundKey) in SystemVerilog for synthesis. • Build a modular RTL design (e.g., separate modules for S-box, key expansion, round logic) to make it reusable and clear.	**Front End Domains Communications**
73.	**TVMAFE709**	**Design and Implementation of 32-Bit MIPS-Based Softcore Processor with Enhanced Instruction Set on FPGA** **Objective:** Implement a 32-bit MIPS Softcore Processor on FPGA	**Front End Domains FPGA**

		• Design a soft (synthesizable) CPU core compatible with the 32-bit MIPS architecture, meant to run on an FPGA. • Provide a verified register file, ALU, control unit, and pipeline (or non-pipeline) stages for executing MIPS instructions.	
74.	**TVMAFE710**	**An FPGA Implementation of a 16-bit Adder for Signed Magnitude Numbers** **Objective:** Implement Arithmetic for Signed-Magnitude Representation • Design a 16-bit adder that correctly handles signed-magnitude numbers, which means correctly processing the sign bit separately from the magnitude bits. •	**Front End Domains Arithmetic Core**
75.	**TVMAFE711, TVMAFE712, TVMAFE713**	**Dot Matrix Interface using FPGA** **Objective:** 1. Design FPGA-Based Controller for Dot Matrix Display • Implement the control logic for a dot matrix LED display using FPGA. • Generate row and column scanning signals (multiplexing) efficiently to drive the matrix. 2. Character / Pattern Generation • Create a memory (e.g., ROM or block RAM) on the FPGA to store predefined dot patterns. • Design logic to read from this memory and output correct bit patterns to display the desired image or text.	**DSP Core, FPGA, Testing**
76.	**TVMAFE714**	**Performance Analysis of MAC Unit with Various Parallel Adders** **Objective:** Evaluate Different Parallel Adders in MAC Context • Analyze how various parallel adder architectures (e.g., Carry Look-Ahead, Carry Select, Carry Save, Carry Skip, Parallel-Prefix adders) affect the performance of a MAC unit.	**Front End Domains Arithmetic Core**

		• Determine which adder type offers the best trade-off of delay, power, and area when used in the accumulation (adder) stage of a MAC.	
77.	**TVMABE374, TVMABE375**	**Sustainable Circuit Design of Energy Efficient 16 bit Counter using Adiabatic Logic** **Objective:** Apply Adiabatic Logic for Energy Efficiency • Use adiabatic (energy-recovery) logic styles to recycle charge instead of dissipating it, thereby greatly reducing dynamic power. • Select a suitable adiabatic logic family (e.g., ECRL, PFAL) for the design to optimize performance and energy saving.	**Back End Domains Low Power VLSI /Transistor Logic**
78.	**TVMAFE715**	**FPGA Based Low Power Approximate Hybrid Parallel Prefix Adders with Less Area** **Objective:** Design Hybrid Parallel Prefix Adders with Approximation • Develop hybrid parallel prefix adder architectures (e.g., combining exact logic in MSBs and approximate logic in LSBs) to balance accuracy and hardware efficiency. • Incorporate approximate prefix operators (AxPOs) or simplified carry logic in least significant portions to reduce complexity.	**Front End Domains Arithmetic Core**
79.	**TVMABE376, TVMABE377, TVMABE378, TVMABE379**	**Design and Implementation of a 4-Bit Carry Select Adder using MTCMOS-Based Ripple Carry Adder with 10T Full Adders in 90nm Technology** **Objective:** Design a Low-Power 10-Transistor Full Adder • Implement a 10-transistor full adder (10 T FA) optimized for low leakage and power consumption. • Use MTCMOS (multi-threshold CMOS) technique to minimize leakage power: employ high-VT transistors in idle paths and low-VT transistors in speed-critical paths. MTCMOS is a known method to reduce leakage in CMOS circuits. • Target the design for 90 nm CMOS technology, ensuring that the transistor sizing and threshold	**Back End Domains Low Power VLSI/Transistor Logic/Nano Technology/Cadence EDA**

		voltage selection are appropriate for that process node.	
80.	TVMABE380, TVMABE381	**Design And Analysis Of High-Performance 16-Bit Hybrid Adder Using Ksa & Hca Adder With Domino Logic** **Objective:** Design a 16-bit Hybrid Parallel-Prefix Adder • Combine Kogge-Stone Adder (KSA) and Han-Carlson Adder (HCA) to create a hybrid parallel-prefix adder. • Leverage the strengths of both: KSA for very low carry propagation delay, and HCA for reduced wiring complexity / area.	**Back End Domains Low Power VLSI/ Cadence EDA**
81.	TVMABE381, TVMABE382, TVMABE383, TVMABE384	**Design and Analysis of Different Adders Using Reversible Logic Gates** **Objective:** Optimize for Low Power / Quantum Cost • Minimize quantum cost (a measure of gate complexity in reversible / quantum circuits). • Reduce the number of "garbage outputs" (unwanted output bits) and "constant inputs" since they contribute to inefficiency. • Explore trade-offs between different adder topologies in terms of quantum cost, delay, and garbage outputs.	**Back End Domains Transistor Logic/Nano Technology/Cadence EDA**
82.	TVMAFE716	**Designing a High-Speed, Low-Area Three-Operand Binary Adder using Kogge-Stone, Han-Carlson, and Ladner-Fischer VLSI Architectures** **Objective:** Leverage Parallel-Prefix Architectures • Explore and design three-operand addition using Kogge-Stone (KS) prefix tree to minimize delay. • Use Han-Carlson (HCA) architecture to balance speed and area — HCA offers a compromise: relatively low depth with less wiring / gate complexity than full Kogge-Stone. • Use Ladner-Fischer (LF) prefix architecture for its low logic-depth and manageable fan-out, aiming to reduce delay and possibly area.	**Front End Domains Arithmetic Core**

83.	TVMABE385, TVMABE386, TVMABE387	**An Energy-Efficient Modified Carry Select Adder Using NCFET for Enhanced Logic Performance** **Objective:** Leverage NCFET Technology for Low-Power Design • Use Negative Capacitance FETs (NCFETs) to design the modified carry-select adder (CSA), taking advantage of NCFET's steep subthreshold slope and low-voltage operation to reduce energy consumption. • Optimize the NCFET device parameters (e.g., ferroelectric layer thickness) to strike a balance between low leakage and high drive current.	**Back End Domains Low Power VLSI/ Transistor Logic/ Cadence EDA**
84.	TVMAFE717, TVMAFE718	**Performance Analysis for Optimized ALU Design Using Carry Select Adder and Vedic Multiplier** **Objective:** Design an Optimized ALU Architecture • Develop a 16-bit (or desired width) Arithmetic Logic Unit (ALU) that uses a Carry Select Adder (CSA) for addition/subtraction operations. • Integrate a Vedic Multiplier (based on Vedic mathematics, e.g., the Urdhva-Tiryakbhyam sutra) for multiplication operations to maximize speed and area efficiency.	**Front End Domains DSP Core/ Arithmetic Core**
85.	TVMABE388, TVMABE389, TVMABE390	**Design and Implementation of High-Speed, Low Power Carry Look-Ahead Adder Using Hybrid GDI Logic and Transmission Gates** **Objective:** Hybrid Logic Style (GDI + Transmission Gates) • Leverage Gate Diffusion Input (GDI) technique to design basic logic functions (e.g., AND, OR, XOR) used in the carry-generator and sum logic, reducing transistor count and power. • Use Transmission Gates (TG) (i.e., complementary pass-transistor structures) where beneficial (e.g., multiplexers, gating logic) to maintain full voltage swing and reduce resistance / delay. • Combine the two logic styles in a "hybrid" way, such that their strengths (GDI's low power, TG's good signal integrity) complement each other.	**Back End Domains Low Power VLSI/ Transistor Logic/ Nano Technology**

86.	TVMAFE719	**Design of Power and Area Optimized 16 – bit Multiplier** **Objective:** Minimize Power Consumption • Design the multiplier architecture to reduce both dynamic and static (leakage) power. • Use low-power design techniques such as power gating, clock gating, or optimized partial-product generation to limit switching activity. • Explore encoding or approximate methods (if acceptable) to further reduce power while maintaining acceptable accuracy.	**Front End Domains Arithmetic Core**
87.	TVMAFE720	**Low Power Pulse Counter with SPI Interface** **Objective:** Integrate SPI Interface for Communication • Provide a Serial Peripheral Interface (SPI) to allow external microcontrollers or systems to read the count value. The SPI interface should support basic read (and optionally write/reset) operations. • Ensure the SPI logic is low-power and does not dominate the overall power budget.	**Front End Domains Communications**
88.	TVMABE391, TVMABE392, TVMABE393	**A Bit-Level Double Counter Enabling Power-Efficient High-Bandwidth VCO-ADCs** **Objective:** Develop a Novel Counter Structure • Design a latch-based, bit-level redundant coarse counter (a "double counter") that can operate reliably at very high VCO (Voltage-Controlled Oscillator) frequencies. • Resolve the asynchrony (timing mismatch) between the coarse counter and fine counter in a coarse-fine VCO-ADC architecture, by enabling fast ambiguity resolution.	**Back End Domains Low Power VLSI/Nano Technology/Cadence EDA**
89.	TVMABE394, TVMABE395, TVMABE396	**Design and Implementation of a Low-Power 4-Bit Synchronous Up Counter Using Gate-Diffusion Input Technology** **Objective:** The primary objective of the project "Design and Implementation of a Low-Power 4-Bit Synchronous Up Counter Using Gate-Diffusion Input (GDI) Technology" is to develop a compact and energy-efficient digital counter	**Back End Domains Low Power VLSI/ Transistor Logic/ Nano Technology**

		architecture by leveraging the GDI logic technique. The design aims to minimize power consumption, reduce transistor count, and achieve improved switching performance compared to conventional CMOS-based counters. Additionally, the project focuses on implementing and validating the proposed 4-bit synchronous up counter through schematic simulation and analyzing key performance metrics such as power dissipation, delay, area, and power–delay product (PDP) to demonstrate the advantages of GDI technology in low-power VLSI applications.	
90.	**TVMABE397, TVMABE398, TVMABE399, TVMABE400**	**Gated Delay Line Up-Down Counters for Mixed-Signal Processing** **Objective:** Design a Gated Delay-Line Based Counter • Develop a novel up-down counter architecture that uses a *gated delay line* to generate timing for count increments/decrements. • Enable fine control over counting by gating the delay line (i.e., enabling or disabling pulses) so that the counter only advances when mixed-signal conditions require it.	**Back End Domains Low Power VLSI/ Transistor Logic/ Nano Technology/ Cadence EDA**
91.	**TVMAFE731**	**Performance Comparison of 16-Bit ALU and 32-Bit ALU Using Verilog** **Objective:** The objective of this project is to design and implement both 16-bit and 32-bit ALUs using Verilog. It aims to compare their performance based on key metrics such as speed, area, and power consumption.	**Front End Domains Arithmetic Core**
92.	**TVMAFE721**	**Breaking XOR Arbiter PUFs With Chosen Challenge Attack** **Objective:** 1. To analyze the structural vulnerabilities in XOR-Arbiter Physical Unclonable Functions (PUFs), particularly how combining multiple arbiter chains affects security against modeling attacks. 2. To study the effectiveness of chosen-challenge attacks (CCA) on XOR-Arbiter PUF variants and understand how selective querying can leak information about the internal delay characteristics.	**Front End Domains Arithmetic Core**

93.	TVMAFE722	**Verilog Code Generation of Hierarchical Design Using LLMs** **Objective:** 1. To explore the capability of Large Language Models (LLMs) in generating accurate and synthesizable Verilog HDL for hierarchical digital designs. 2. To evaluate the efficiency and reliability of LLM-generated Verilog code compared to manually written RTL in terms of correctness, modularity, and hardware resource utilization.	**Front End Domains Finite State Machines**
94.	TVMAFE722, TVMAFE723	**Implementation of Low-Density Parity-Check (LDPC) Codes in Verilog HDL** **Objective:** 1. To understand the structure and properties of LDPC codes and their advantages in error correction for digital communication systems. 2. To design and implement LDPC encoder and decoder modules in Verilog HDL for efficient hardware realization.	**Front End Domains Testing/DSP Core**
95.	TVMAFE726, TVMAFE724, TVMAFE725	**VLSI design of 128-point finite field FFT multiplier** **Objective:** 1. To study the principles of finite field arithmetic and its application in digital signal processing, particularly in Galois fields (GF) for FFT computations. 2. To design a 128-point Fast Fourier Transform (FFT) architecture optimized for finite field multiplication in hardware.	**Front End Domains DSP Core/Arithmetic Core/Testing**
96.	TVMAFE727	**Evaluating the Differences Between Sequential and Combinational Logic Circuit Designs** **Objective:** 1. To understand the fundamental concepts of combinational and sequential logic circuits, including their operational principles and timing behaviors. 2. To design representative combinational circuits (e.g., adders, multiplexers, decoders) and sequential circuits (e.g., flip-flops, counters, shift registers) for comparison.	**Front End Domains Arithmetic Core**
97.	TVMAFE732	**Revamping Verilog Semantics for Foundational Verification** **Objective:** The objective of this project is to revamp the semantics of Verilog to address challenges in modern	**Front End Domains** **DSP Core**

		verification processes. By refining the language's syntax and semantics, the project aims to improve its expressiveness and precision for complex digital system design. The goal is to enhance the verification capabilities, making it easier to validate the correctness of hardware descriptions. The project also seeks to introduce new methodologies for error detection, reducing verification time and effort. Ultimately, this will improve the reliability and efficiency of hardware designs using Verilog in foundational verification tasks.	
98.	**TVMABE401, TVMABE402, TVMABE403**	**Photonic Crystal-Based D Flip-Flops for Ultrafast Sequential Circuit Applications** **Objective:** 1. To study the fundamentals of photonic crystals and their unique properties, such as bandgap engineering and light manipulation, for use in optical computing. 2. To design D flip-flops using photonic crystal structures, enabling ultrafast switching and sequential logic operations without relying on traditional electronic transistors.	**Back End Domains Low Power VLSI/Transistor Logic/Nano Technology**
99.	**TVMAFE728**	**RASC: A Low-Power Reconfigurable 4-2 Adder-Subtractor-Compressor** **Objective:** 1. To study the design principles of arithmetic circuits, particularly adders, subtractors, and compressors, and understand their role in high-speed digital systems. 2. To design a 4-2 adder-subtractor-compressor module that is reconfigurable, allowing the circuit to perform addition, subtraction, or compression operations based on control signals.	**ront End Domains Arithmetic Core**
100	**TVMAFE729**	**Low Latency based Floating Point Multiplier using Parallel Prefix Adders** **Objective:** 1. To study the principles of floating-point arithmetic and the importance of efficient multiplication in high-performance computing and digital signal processing applications. 2. To design a floating-point multiplier architecture that reduces latency by using parallel prefix adders for fast partial product summation.	**Front End Domains Arithmetic Core**

101	TVMAFE730	**Approximate Adders for Efficient Circuits: Advantages and Limitations Compared to RCA** **Objective:** 1. To study the design principles of approximate adders and understand how they trade off computational accuracy for improvements in power, area, and speed. 2. To implement and analyze different types of approximate adder architectures, such as truncated adders, speculative adders, and error-tolerant designs.	**Front End Domains Arithmetic Core**
102	TVMABE404, TVMABE405, TVMABE406	**Reliable Multistate RRAM Devices for Reconfigurable CAM and IMC Applications** **Objective:** The objective of this work is to design and evaluate reliable multistate Resistive Random-Access Memory (RRAM) devices for use in reconfigurable Content-Addressable Memory (CAM) and In-Memory Computing (IMC) architectures. The study aims to achieve stable multi-level resistance states, improved endurance, low write variability, and robust switching behavior, enabling energy-efficient and high-density hardware for next-generation data-intensive and AI-driven computing systems.	**Back End Domains Low Power VLSI/Transistor Logic/Cadence EDA**
103	TVMABE407, TVMABE408, TVMABE409, TVMABE410	**An Ultra-Low-Power Fully-Static Contention-Free Single-Phase-Clock Flip-Flop With Low Area** **Objective:** To design and demonstrate a flip-flop architecture that: • Consumes ultra-low power, especially by minimizing clock power and switching activity • Is fully static, eliminating leakage and data loss issues found in dynamic or semi-dynamic flip-flops • Is contention-free, avoiding short-circuit current during clock transitions • Operates using a single-phase clock, reducing clocking complexity and clock-tree power	**Back End Domains Low Power VLSI/Transistor Logic/Cadence EDA/ Nano technology**

		• Achieves these benefits with a small silicon area, making it suitable for dense VLSI and low-power application	
104	**TVMABE411, TVMABE412, TVMABE413, TVMABE414**	**A High-Accuracy Bandgap Reference with Compact Output Driver** **Objective:** To design a bandgap reference (BGR) circuit that: • Provides high output voltage accuracy across process, voltage, and temperature (PVT) variations • Achieves low temperature coefficient for stable reference voltage • Integrates a compact, area-efficient output driver capable of driving loads without significant voltage drop • Reduces power consumption while maintaining precision • Minimizes silicon area and complexity, making it suitable for highly integrated ICs	**Back End Domains Low Power VLSI/Transistor Logic/Cadence EDA/ Nano technology**
105	**TVMABE415, TVMABE416, TVMABE417, TVMABE418**	**Comparative Analysis of 8T, 10T, and 12T Realistic CNTFET Based SRAM** **Objective:** To evaluate and compare the performance of 8T, 10T, and 12T SRAM cell architectures implemented using realistic CNTFET models in order to: • Analyze read and write stability (Static Noise Margin) • Compare power consumption, including leakage and dynamic power • Study area overhead and transistor count trade-offs • Assess read/write delay and reliability at scaled technology nodes • Examine robustness to process variations and low-voltage operation	**Back End Domains Low Power VLSI/Transistor Logic/Cadence EDA/ Nano technology**

106	TVMABE419, TVMABE420, TVMABE421, TVMABE422	**Performance Analysis of 8-bit, 16-bit, 32-bit and 64-bit ALUs with CMOS-Based Reversible Gates Using Advanced Power Reduction Techniques** **Objective:** To design and analyze Arithmetic Logic Units (ALUs) of varying word lengths (8-bit, 16-bit, 32-bit, and 64-bit) using CMOS-based reversible logic gates, in order to: • Reduce power dissipation, particularly switching and leakage power, using advanced power-reduction techniques • Evaluate and compare performance parameters such as power consumption, delay, and area across different ALU sizes • Demonstrate the scalability and effectiveness of reversible logic for higher-bit-width ALU implementations • Analyze the impact of advanced power optimization techniques on overall ALU efficiency	**Back End Domains Low Power VLSI/Transistor Logic/Cadence EDA/ Nano technology**
107	TVMAFE733, TVMAFE734	**Advanced Adaptive Median Filter for Reducing Salt-and-Pepper Noise in GPR Data** **Objective:** To develop and evaluate an advanced adaptive median filtering technique that: • Effectively removes salt-and-pepper noise from Ground Penetrating Radar (GPR) data • Preserves important subsurface features, such as layer boundaries and target reflections, without blurring edges • Adapts filtering parameters based on local data characteristics to improve noise reduction performance • Enhances the signal-to-noise ratio (SNR) and overall interpretability of GPR images • Outperforms conventional median and standard adaptive median filters in terms of accuracy and detail preservation	**Front End Domains/ Finite State Machines/DSP Core**

108	TVMABE440	**Comparative Analysis of XOR Implementation using CMOS Logic and Domino Logic** **Objective:** The paper aims to compare the implementation of the XOR logic function using two different CMOS-based circuit design styles — namely CMOS static logic and domino logic with a keeper technique. The study focuses on evaluating these XOR gate implementations in terms of key performance metrics (such as power consumption, delay, transistor count, and overall logic performance) to determine which logic style offers better efficiency and suitability for VLSI designs.	**Back End Domains Low Power VLSI**
109	TVMABE441, TVMABE442	**A Two-Stage CMOS Amplifier with High Degree of Stability for All Capacitive Loads** **Objective:** A Two-Stage CMOS Amplifier with High Degree of Stability for All Capacitive Loads" is to design and demonstrate a two-stage CMOS amplifier that remains unconditionally stable for any value of capacitive load. The work aims to overcome the traditional stability limitations of conventional two-stage amplifiers by introducing a compensation technique that generates a left-half-plane zero, which effectively tracks or cancels the output pole under varying load conditions. By doing so, the amplifier achieves stable operation similar to a single-pole system across process, voltage, temperature, and load variations, making it highly suitable for robust VLSI and analog integrated circuit applications.	**Back End Domains Low Power VLSI/ Transistor logic**
110	TVMAFE764, TVMAFE765	**Power and Area Optimized Data Path Unit for A RISCV Processor** **Objective:** The primary objective of "Power and Area Optimized Data Path Unit for A RISC-V Processor" is to design and implement a data path architecture for a RISC-V processor that minimizes both silicon area and power consumption without significantly degrading performance. This work focuses on optimizing the internal data path components — such as the ALU, register file, and pipeline interconnections — to achieve an efficient balance between energy efficiency and hardware resource usage. By leveraging microarchitectural techniques (e.g., narrowed datapaths, hardware sharing, and simplified	**Front End Domains Arithmetic Core/ DSP Core**

		control logic), the design aims to reduce dynamic switching and static leakage, making it suitable for resource-constrained embedded and IoT applications that require low power yet effective computational capability.	
111	TVMABE443	**Design and Investigation of a Delay-Controlled 8-Bit ALU** **Objective:** The primary objective of "Design and investigation of a delay controlled ALU employing FinFET & CNTFET technologies" is to develop and evaluate a reconfigurable arithmetic logic unit (ALU) with controllable delay characteristics that achieves improved performance over conventional ALUs. This research focuses on integrating novel full-adder structures—such as Carry Output Predicted Adders (COPA) and Carry Input Selective Adders (CISA)—with FinFET and Carbon Nanotube Field Effect Transistor (CNTFET) technologies to construct a delay-controlled ALU that can perform arithmetic and logical operations with reduced power consumption and latency. Through simulation on an 18 nm process using Cadence Virtuoso, the design demonstrates significantly lower power usage and delay compared to traditional implementations, making it suitable for low-power, high-efficiency digital circuit applications.	**Back End Domains** **Low Power VLSI**
112	TVMAFE767, TVMAFE766	**A High-Speed, Energy-Efficient Wallace Tree Multiplier Using Reversible Counters** **Objective:** The objective of a study titled "A High-Speed, Energy-Efficient Wallace Tree Multiplier Using Reversible Counters" would be to design, analyze, and implement a Wallace tree multiplier architecture that uses reversible counter modules to reduce power consumption, area overhead, and delay compared to conventional Wallace tree multipliers. The research typically focuses on leveraging reversible logic principles to minimize energy dissipation during multiplication operations — a critical requirement in low-power and high-performance digital systems such as DSP and embedded processors. By introducing reversible counters in the partial product reduction stages, the design aims to improve computational speed and energy efficiency, making it	**Front End Domains** **Arithmetic Core/** **Communication**

		suitable for modern VLSI applications where reduced power and high throughput are essential.	

PROJECT SUPPORTS FOR STUDENTS:

- PROJECT ABSTRACT
- PROJECT IEEE BASE PAPER/ REFERENCE PAPER
- PROJECT PRESENTATION IN PPT FORMAT
- PROJECT REVIEW ASSISTANCE FOR VIVA
- PROJECT DIAGRAMS
- PROJECT SOURCE CODE
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